UNIVERSITA' DEGLI STUDI DI SALERNO

DEPARTMENT OF PHYSICS "E. R. CAIANIELLO"

DOCTOR OF PHILOSOPHY IN PHYSICS

XXXII CICLO (2016-2019)

Ph.D. Thesis in

GRAPHENE/SILICON SCHOTTKY DIODE

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ACADEMIC YEAR 2019/2020

Abstract

In this works we fabricated four graphene/silicon heterojunctions, which differ for structure and substrate type, and performed electrical and optical characterization. The first device was realized by depositing a layer of graphene on a trench patterned low n-doped silicon substrate. We obtained a graphene/silicon Schottky diode connected in parallel with a graphene/oxide/silicon MOS (Metal Oxide Semiconductor) capacitor. The device shows a rectification factor of 3 orders of magnitude and a Schottky barrier of $0.56\ eV$. The device displays a reverse current greater than the forward one when exposed to white LED light. We explained this phenomenon by taking into account the MOS capacitor connected in parallel which act as a reservoir of charges. The second device presents the same structure, but a low p-doped silicon substrate was used. In this case, we obtained a Schottky barrier of $0.17\ eV$ which tends to get smaller when annealed to high temperature. This behaviour has been attributed to the boron atoms which diffuse from the silicon to graphene inducing a p-doping, which further reduce the Schottky barrier. The third device was realized by depositing a graphene layer on a pillar-patterned high n-doped silicon substrate. The device shows a Schottky barrier of $0.11\ eV$ and a reverse current which grows exponentially respect to the bias. We explained this result by considering the pillar structure which, magnifying the electric field around its corners, favours the up-shift (down-shift) of the graphene Fermi level reducing (or increasing) the Schottky barrier upon application of a bias. At higher temperature this behaviour tends to disappear since the Schottky barrier variations are overcome by the thermal effects. The last device was fabricated by depositing a graphene layer on a matrix of silicon tips. The device shows a Schottky barrier of $0.36\ eV$ which corresponds to a rectification factor of almost three orders of magnitude and a reverse current which grows exponentially with the bias over the whole temperature range. Similar to the previous junction, the tip geometry magnifies the electric field and allows to tune the Schottky barrier by changing the bias. The device shows an ideality factor closer to the unity meaning that the tip geometry reduces the formation of inhomogeneity, which can affect the junction properties, and allows the formation of higher Schottky barrier.

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Introduction

In the last decades, the growing demand of fastest and smallest devices has pushed the scientific community to look for a new non silicon-based technology. This technology has yet to be invented, but the discovery of the bidimensional materials, such as graphene [1], MoS_2 [2,3], WSe_2 [4,5] and phosphorene [6], etc. could be a good starting point for its achievement.

Of all bidimensional material, graphene looks like the most promising one. Theorized by Philip Wallace, which studied its band structure in 1947 [7], it was firstly produced by the chemist Hans-Peter Bohen in 1962 from graphene oxide. Because of the high fabrication cost and difficulty to obtain high quality monolayer, graphene could not spark the interest of the scientific community. It was only in 2004 when Prof Geim and Prof. Novoselov were able to obtain high-quality graphene monolayer from graphite using, what is usually referred now as the "scotch tape" method [1]. Later, new fabrication methods were discovered. Graphene layer can be grown from silicon carbide or by chemical vapour deposition (CVD) using carbon-based gas [8]. The possibility to realize large area high-quality monolayer and the compatibility with the integrated circuit fabrication process has attracted great interest as graphene could be the first step in the direction to realize the new technology that the scientific community is looking for [9].

Graphene can carry higher density current than copper, possesses higher carrier mobility than silicon [10], is stronger than steel [11], can form low contact resistance [12–14] and has low optical absorption coefficient [15] and offers the largest possible contact area which makes it an ideal platform for sensing applications. Because of its conic bandgap-less structure [7,16,17], graphene can absorb light across a broad spectrum, from the UV to the IR wavelengths [15,18]. All these properties make it suitable to realize a new generation of semiconductor devices starting from transistors [13,19–25] to Schottky diodes [16,26–32], photodetectors, solar panels [9,15,33–38] and chemical sensors [39–41].

Graphene/Silicon (Gr/Si) heterojunctions are the simplest device that can be realized. One of the first graphene/SiC Schottky junction was realized and characterized in 2009 by Filippo Giannazzo from the National Research Council in Catania, Italy, and his group [42]. And the next year Xinming Li from Beijing University and his group realized Gr/Si Schottky solar cell using CVD grown graphene on a silicon substrate [43]. Chun-Chung Chen from California University et al. realized two Gr/Si Schottky diodes by transferring mechanically exfoliated graphene on a n- and p-doped silicon substrate [26]. Later, a Gr/Si diode was realized by transferring CVD grown graphene on p-silicon substrate by Y. An et al. [44].

Gr/Si junctions offer the opportunities to study the physics occurring at the interface between a 2D and a 3D material, as well as, between a zero and a defined bandgap system and it can be the platform to investigate electronic properties and transport mechanism. Because of the graphene semimetallic behaviour, Gr/Si heterojunction current-voltage (I-V) characteristic shows a rectification behaviour which can be roughly described using the ideal diode equation. In fact, Gr/Si shows a higher saturation current density than a commercial Schottky diode [45,46]. As, we will see later, this behaviour is due to the absence of the band gap and the low-density state close to the Dirac point. The possibility to control the Schottky barrier

formed at the Gr/Si interface can be exploited to realize tunable photosensor able to detect wider wavelength range than traditional diodes.

In this work I present the results of four selected Gr/Si Schottky diodes which were realized in collaboration with the Innovation for High Performance (IHP) Microelectronics centre in Frankfurt Oder, Germany. The devices were chosen based on their I-V characteristic, optical response and substrate doping and geometry.

This work is structured in the following way: In the first chapter, I will describe graphene properties. I will briefly discuss graphene electronic properties focusing on its honeycomb lattice, band structure and electrical conductivity. Then I will describe the most common way used to dope a graphene layer and its optical properties. I will conclude the chapter discussing the different methods used to fabricate graphene monolayer and how to transfer it on a substrate.

In the second chapter, I will cover the physical phenomena and the current transport mechanism in a metal/n-doped semiconductor junction. I will conclude by describing the most common methods used to determinate all the Schottky parameters.

In the third chapter I will start by introducing the Gr/Si junction band structure, the model firstly introduced by S. Tongay to described the junction I-V characteristic [46] and then I will conclude by briefly discussing the optical properties of the junction.

After that, I will introduce the two Gr/Si planar junctions that I have been studying.

The first Gr/Si planar junction was fabricated starting from a low n-doped silicon substrate on which an oxide layer was deposited by CVD. A strip of few micrometres was patterned by lithography and a graphene monolayer large enough to cover part of the strip and the oxide was deposited on the top. I-V characteristics were measured at different temperature and in low vacuum, and at different illumination levels. The Gr/n-Si planar junction shows a Schottky barrier of 0.46 eV in agreement with the one reported in literature. The novelty of the junction is the photocurrent which is higher than the forward current at high intensity illumination level. The high photocurrent is due to the graphene/oxide/semiconductor heterostructure which acts as a metal/oxide/semiconductor (MOS) capacitor. The MOS capacitor attract the photogenerated charge between the semiconductor and the oxide layer forming a reservoir which contributes to the Gr/Si photocurrent. This hypothesis has been later confirmed by other groups [33,34].

The second Gr/Si planar junction was fabricated in the same way of the previous one, but a low p-doped silicon substrate was used. The Gr/p-Si junction possesses a Schottky barrier of 0.11 eV. The low Schottky barrier is the result of the junction between two p-doped semiconductors. When graphene is exposed to the atmosphere, it shows a p-doped behaviour thus the Fermi level is shifted down the Dirac point and close to the silicon valence band. Also, we observed a reduction of the Schottky barrier and of the rectification factor after the annealing treatment at 400 K. This degradation is due to the boron atom in the silicon substrate and the graphene lattice inhomogeneity. The boron atoms are weakly bonded to the silicon ones and when enough energy is given to the system, in this case by raising the system temperature, they can out-diffuse and place themselves in the graphene lattice. The boron atoms p-dope the graphene and shift its Fermi level further down reducing the Schottky barrier [47].

In the last chapter, I will show the result obtained by characterized two graphene patterned silicon junctions. In the first Gr/Si patterned junction, three pillars with different size and the same size were patterned on a high doped silicon substrate. An oxide layer was CVD grown until it covered the pillar and it was then partially removed by CMP (Chemical-Mechanical Polishing) until the pillars surface were exposed. The I-V characteristic was measured at different temperature in low vacuum. The junction displays a constant reverse saturation current respect the bias at high temperature, while at lower temperature the saturation current grows exponentially with the bias. This behaviour can be explained by taking into the account the graphene low density of states. The application of a negative (or positive) bias makes the graphene Fermi level shift up (or down) and thus it reduces (or increases) the Schottky barrier. This phenomenon is not visible at higher temperature since the charges possess higher energy and can easily overcome the barrier showing a constant reverse current. Also, the substrate geometry enhances this behaviour: The pillar corners magnify the electric field and induce a stronger potential on the graphene, thus modifying the Schottky barrier [32].

The second device was realized to confirm what we observed in the previous one. From a highly doped silicon substrate a matrix of $\sim 500\,nm$ height tips were patterned and then covered with a CVD grown oxide layer. The silicon tips were then subjected to CMP till revealing a circular surface with a diameter of $50\,nm$. Finally, a commercial graphene monolayer was transferred on the top. The Gr/Si-tip I-V characteristics were measured at different temperature and in low vacuum. The Gr/Si-tip saturation current grows exponentially at each temperature. We determined the Schottky barrier at different bias and we observed a linear increase with respect to the bias. This result confirmed what we expected from the study of the graphene on Si pillars and suggested that more performant and high-quality Gr/Si junctions can be achieved by reducing the junction surface and by using a sharper geometry [28].

In summary, in this work, I fabricated and characterized different Gr/Si junctions and studied how the doping and the geometry of the substrate affects the I-V characteristics and Schottky barrier. I observed that a Gr/p-Si diode displays a low rectification and tends to degrade at higher temperature, while a Gr/n-Si diode shows a rectification of 4 order of magnitude and withstands higher temperatures. Both devices display a photocurrent almost higher than the forward current due to the MOS capacitor connected in parallel with the Gr/Si Schottky diode. This result is very interesting since both devices were not fabricated for photodetection and gives a clue on how to increase Gr/Si photo-sensitivity. We observed also that it is possible to tune the Schottky barrier height by patterning the substrate with a pillar or a tip geometry, which enable better control of the Schottky barrier height. The possibility to tune the Schottky barrier allows to detect different light wavelengths. These results could be the milestone to produce a new generation of cheaper tunable high sensible photodetectors.

1 Graphene

1.1 Introduction

Carbon is one of the most versatile elements in nature, it can form different compounds by establishing different types of bonds. Carbon ground state electronic configuration is $1s^2 2s^2 2p^2$ and possesses four valence electrons, $2s$ and $2p$. Since two unpaired $2p$ electrons are present, Carbon tends to maximize the number of bonds by rearranging the configuration of the valence electrons. Such rearrangement is known as hybridization and only the $2s$ and $2p$ electrons are affected. One of the $2s$ electrons is promoted in the $2p$ orbital creating an excited state. Below, I will briefly describe the three hybridization possible configurations.

The $2s$ and $2p$ orbitals can mix in order to form three different hybrid orbitals. One possible hybridization consists in the formation of four sp^3 orbitals each filled with one electron (Fig. 1 (a)). In order to reduce the repulsion between them, the hybrid orbitals arrange themselves in a tetrahedral geometry and form four σ bonds with an angle of $109.5°$ with the nearest carbon atoms. Carbon atoms in this configuration can be found in diamond and Methane (CH_4).

Carbon's orbitals can also mix forming three sp^2 hybrid orbital each filled with one electron (Fig. 2 (b)). These orbitals are arranged in a triangular planar shape with an angle of $120°$ and form three σ bonds with the nearest carbon atoms. The remaining p orbital is perpendicular to this plane and forms π bond by overlapping with the p orbital of another carbon atom outside of the plane. Ethylene (C_2H_4) and benzene (C_6H_6) are typical example of sp^2 hybridization.

The last possible hybridization consists in the formation of two sp orbitals formed by the mixing of the $2s$ orbital and one of the $2p$, each of them filled with one electron (Fig. 1 (c)). The geometry is linear with an angle of $180°$ between each orbital. The carbon atoms in this configuration are bound with the two nearest atoms by one σ bonds and the two π bonds formed by the two unmixed p orbitals.

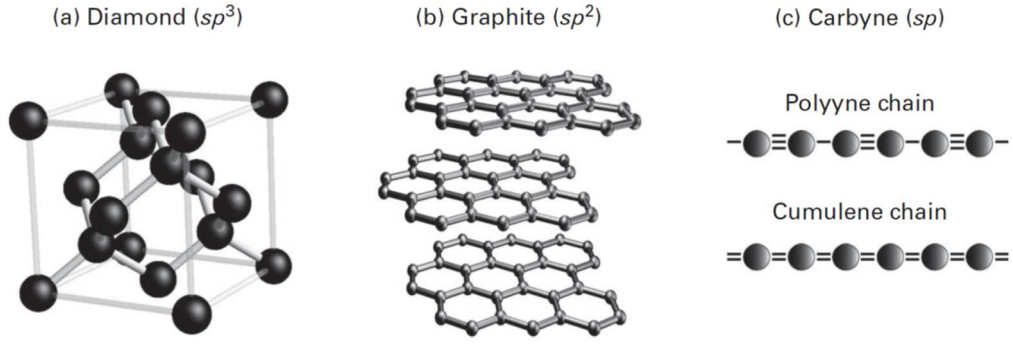


Fig. 1 Carbon structure exhibiting different hybridization: (a) diamond (sp^3); (b) graphite (sp^2); and (c) carbine (sp).

The sp^2 hybridization is the one, which interests us the most. It exhibits a great variety of allotropes, from low-dimensional fullerenes, nanotubes and graphene nanoribbons, to two-

dimensional monolayer graphene, or stacked graphene multilayer. Of all of them, Fig. 2, graphene is the one on which the scientific community has been focused most of its attention in the last years because of its very interesting properties.

Graphene monolayers were first isolated in 2004 by Prof. Novoselov and Prof. Geim from bulk graphite by exfoliation (this technique is known as the "scotch tape method") [1], a discovery which was awarded with the Nobel Prize in 2010.

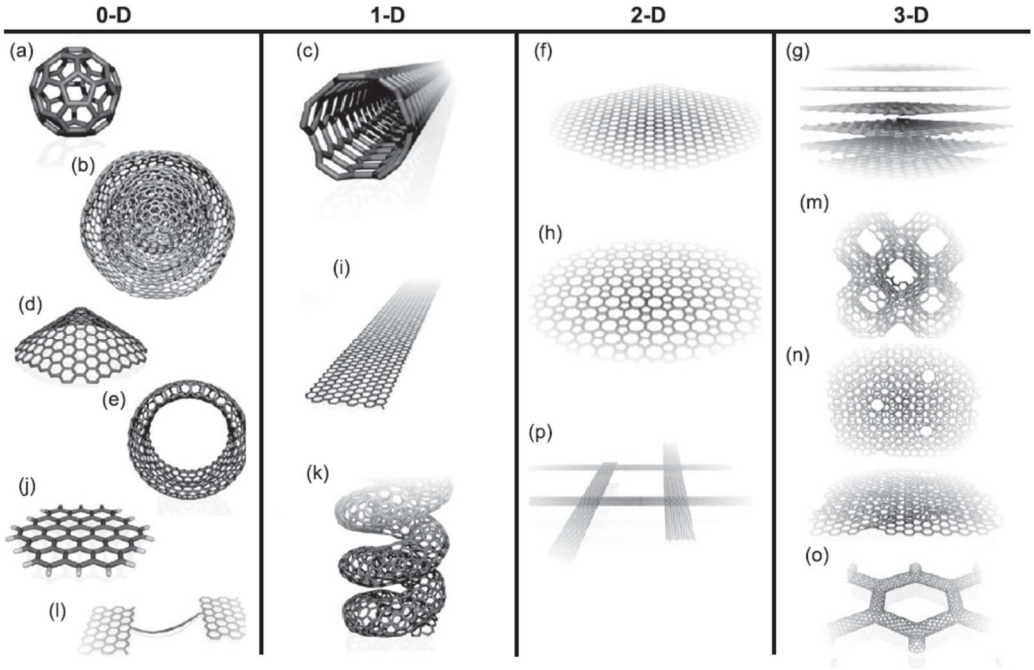


Fig. 2 Atomistic models of various sp^2-like hybridized carbon nanostructures exhibiting different dimensionalities, 0D, 1D, 2D e 3D: (a) C60: buckminsterfullerene; (b) nested giant fullerenes or graphitic onions; (c) carbon nanotube; (d) nanocones or nanohors; (e) nanotorroids; (f) graphene surface; (g) 3D graphite crystal; (h) Haeckelite surface; (i) graphene nanoribbons; (j) graphene clusters; (k) helicoidal carbon nanotube; (l) short carbon chains; (m) 3D Schwarzite crystals; (n) carbon nanofoams (interconnected graphene surface with channels); (o) 3D nanotube network, and (p) nanoribbon 2D network

Graphene possesses higher electron mobility than silicon, higher electrical conductivity than the copper and a low optical coefficient [10,16,18,48]. All these properties make the graphene the perfect candidate to realize a new generation of faster electronic devices such as transistors [12,13,22–24], diodes [27–32,49], chemical-biological sensors [39–41], more sensitive photosensors, and cheaper solar panels [9,15,34–38].

In this chapter we will briefly describe the graphene electrical properties, from its band structure to its electrical conductivity. We will also focus on its optical properties and fabrication methods.

1.2 Graphene electronics properties

Graphene is a bidimensional material composed of carbon atoms arranged in a honeycomb lattice. This structure is characterized by two type of bonding within the sp^2 hybridization,

the $2s$, $2p_x$ and $2p_y$ combine to form the inplane σ and the σ^* orbital while the p_z orbital is perpendicular to the plane and forms with p_z neighbouring orbital π and π^* (Fig. 3 (a)). The σ bonds are strongly covalent bonds and are the ones responsible for the graphene mechanical properties. The difference in energies between them is greater than $12\ eV$ so their contributions to the electrical properties can be disregarded (Fig. 3 (b)). Thus, the π orbitals are the only one responsible for the electronic properties.

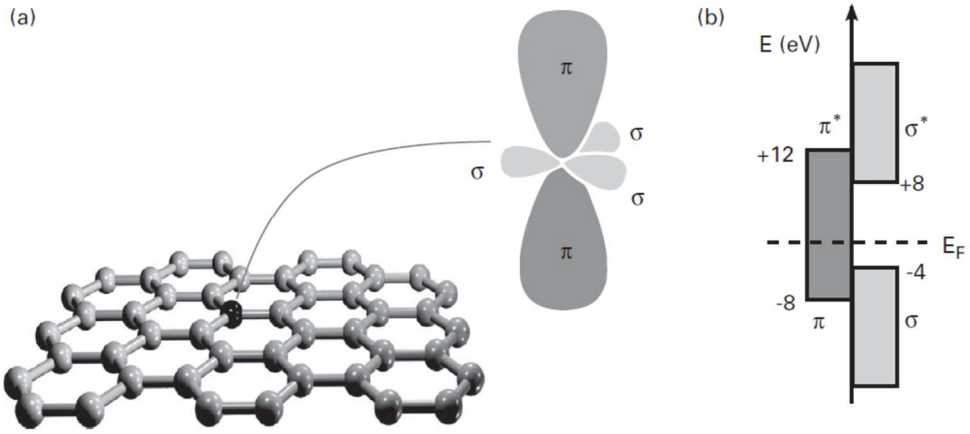


Fig. 3 The carbon valence orbitals. (a) The three σ orbitals in graphene and the π orbital perpendicular to the sheet.

Graphene structure cannot be directly associated with a Bravais lattice. In order to determinate its electrical properties, we will consider the unit cell composed of two atoms. By doing so, we obtain a triangular Bravais lattice, Fig. 4 (a), whose basis vector are defined as

$$\vec{a}_1 = a\left(\frac{\sqrt{3}}{2}, \frac{1}{2}\right), \qquad \vec{a}_2 = a\left(\frac{\sqrt{3}}{2}, \frac{1}{2}\right) \tag{1.1}$$

where $a = \sqrt{3}a_{cc}$ where $a_{cc} = 1.42$ Å is the distance between two carbon atoms. By using the condition $\vec{a}_i \cdot \vec{b}_j = 2\pi\delta_{ij}$ the reciprocal lattice vectors $\left(\vec{b}_1, \vec{b}_2\right)$ can be obtained,

$$\vec{b}_1 = b\left(\frac{1}{2}, \frac{\sqrt{3}}{2}\right), \qquad \vec{b}_2 = b\left(\frac{1}{2}, \frac{\sqrt{3}}{2}\right), \tag{1.2}$$

with $b = 4\pi/3a_{cc} = 4\pi/a\sqrt{3}$ (Fig. 4 (b)). The graphene reciprocal lattice is also a hexagonal lattice but is rotated by 90°. Two corners out of six are inequivalent, the other can be written as one of these two plus a reciprocal lattice vector. These points are denoted K_+ and K_-:

$$\vec{K}_+ = \frac{4\pi}{3a}\left(\frac{\sqrt{3}}{2}, \frac{1}{2}\right), \vec{K}_- = \frac{4\pi}{3a}\left(\frac{\sqrt{3}}{2}, \frac{1}{2}\right) \tag{1.3}$$

The dispersion relation $E\left(\vec{k}\right)$ is obtained from the tight-binding Hamiltonian

$$\mathcal{H}(\vec{k}) = \begin{pmatrix} 0 & -\gamma_0(1 + \exp(i\vec{k}\cdot\vec{a}_1) + \exp(i\vec{k}\cdot\vec{a}_2)) \\ c.c. & 0 \end{pmatrix}. \tag{1.4}$$

where $\gamma_0 \approx 2.7eV$ is the nearest-neighbor hopping interaction between A and B sites and $c.c.$ is the complex conjugate of the off-matrix element.

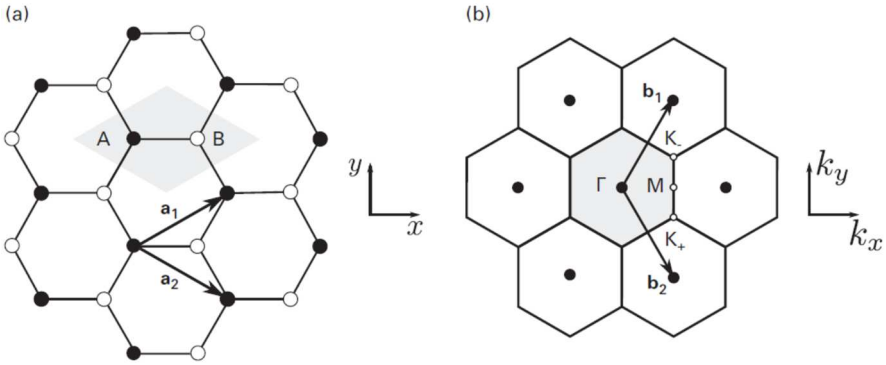


Fig. 4 Showing basis vector $\vec{a}_1$ and $\vec{a}_2$ in the hexagonal network of graphene. This network is a triangular Bravais lattice with a two tom-basis: A (full dots) and B (empty dots). (b) The reciprocal lattice points corresponding to the triangular Bravais lattice (full dots) as well as the associated basis vector $\vec{b}_1$ and $\vec{b}_2$.

By diagonalizing $\mathcal{H}(\vec{k})$ the energy relation is obtained:

$$\begin{aligned} E_{\pm}(\vec{k}) &= \pm\gamma_0|\alpha(\vec{k})| \\ &= \pm\gamma_0\sqrt{3 + 2\cos(\vec{k}\cdot\vec{a}_1) + 2\cos(\vec{k}\cdot\vec{a}_2) + 2\cos\left(\vec{k}\cdot(\vec{a}_2 - \vec{a}_1)\right)} \end{aligned} \tag{1.5}$$

Which can be further expanded:

$$E_{\pm}(k_x, k_y) = \pm\gamma_0\sqrt{1 + 4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{k_y a}{2}\right) + 4\cos^2\left(\frac{k_y a}{2}\right)}. \tag{1.6}$$

The wavevectors $\vec{k} = (k_x, k_y)$ are chosen within the first hexagonal Brillouin zone. In the point $\vec{K}_+$ and $\vec{K}_-$, the function $\alpha(\vec{k}) = 0$ and corresponds to the point where the two bands meet with each other, Fig. 5. By expanding equation (1.6) for $\vec{k}$ in the vicinity of K_+ (or K_-), $\vec{k} = \vec{K}_+ + \vec{q}$ ($\vec{k} = \vec{K}_- + \vec{q}$) a linear dispersion relation is obtained:

$$E_{\pm}(\vec{q}) = \pm\hbar v_F|\vec{q}| \tag{1.7}$$

where

$$v_F = \frac{\sqrt{3}\gamma_0 a}{2\hbar} \tag{1.8}$$

is the group velocity. Equation (1.7) states that the valence and the conduction band possess a conical shape the vertices of which meet at the Fermi level in six points, known as Dirac points, Fig. 5. Close to them, the electrons behave like massless Dirac fermions and their group velocity reaches the value of $v_F \sim 8.5 \times 10^5 m/s$.

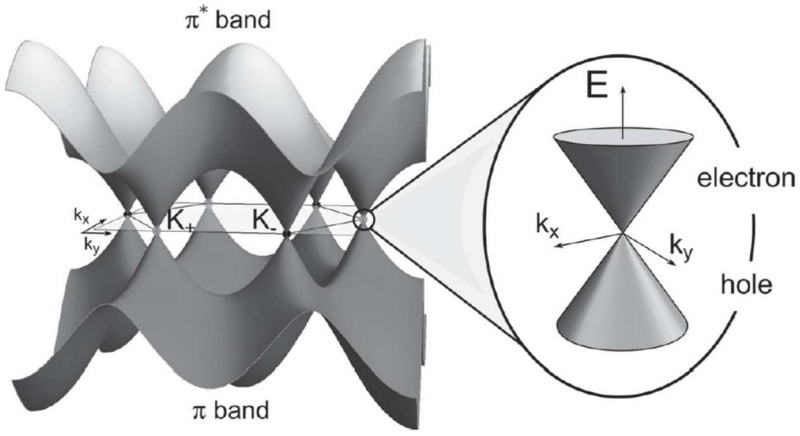


*Fig. 5 Graphene π and π*electronic bands. In this simple approach, the π and π* bands are symmetric with respect to the valence bands. The linear dispersion relation close to K_+ and K_- points of the first 2D Brillouin zone gives rise to the "Dirac cones" a shown on the right*

1.3 Graphene conductivity and mobility

The mobility and the conductivity in graphene depend on the microscopic scattering processes that occur in graphene at a given temperature [50–52]. For ideal and neutral graphene, the E_F is at Dirac point where $n \approx 0$. The position of the Fermi level above or below the Dirac point makes graphene a n- or p-doped semiconductor. In order to determinate the relation between the E_F and n, let us consider the number of states between q and $q + dq$, which is

$$N(q)dq = \frac{Aqdq}{2\pi} \cdot t \tag{1.9}$$

where A is the graphene surface where the number of states is calculated and $t = 2$ is the valley degeneracy. Using the dispersion relation equation (1.7):

$$N(q)dq = N(E)dE = Ag\frac{EdE}{\pi(\hbar v_F)^2} \tag{1.10}$$

by defining the density of states per energy and area $g(E) = N(E)/A$, we obtain

$$g(E) = \frac{2|E|}{\pi\hbar^2 v_F^2} = g_0|E| \tag{1.11}$$

and

$$n = \int_0^\infty g(E)f(E)dE = \frac{2}{\pi}\left(\frac{kT}{\hbar v_F}\right)F_1\left(\frac{E_F}{kT}\right) \approx \frac{1}{\pi}\left(\frac{E_F}{\hbar v_F}\right)^2 \; at\; T = 0K \tag{1.12}$$

where $f(E)$ it is the Fermi function and $F_1\left(\frac{E_F}{kT}\right)$ is the Fermi Dirac integral. Equation (1.12) states that the Fermi level changes as the square of the carrier density:

$$E_F = \mp\frac{h}{2\sqrt{\pi}}v_F\sqrt{n} \tag{1.13}$$

The $(-)$ and $(+)$ sign correspond to p- and n-type graphene respectively. It is also possible to shift the Fermi level using different chemicals, as we will see later.

Now that we know the relation between the E_F and n we can determinate the relation between the energy and the conductivity. Let us consider the case in which the E_F is away from the Dirac point and the carrier density is high. The presence of inhomogeneity or other disorder act as scattering point and reduce the electron mean free path length l. If L is the graphene length, we can distinguish two transport regimes. In the case $l > L$, the transport is ballistic, and the carriers travel from one side to the other of graphene at Fermi velocity v_F. In the other case, $l < L$, the carrier undergo elastic and anelastic collisions, this regime is known as diffusive. Both situation can be described using the Landauer formalism [53].

$$\sigma = \frac{L}{W}\frac{2e^2}{h}\int_0^{\infty} T(E)M(E)\left(-\frac{\partial f}{\partial E}\right)dE \tag{1.14}$$

where W is the width of the graphene, $T(E)$ is the transmission function which value depend on the transport regime, and $M(E)$ is the number of conduction channels. For ballistic transport

$$T(E) = 1 \tag{1.15}$$

while for diffusive:

$$T(E) = \frac{\lambda(E)}{\lambda(E) + L} \tag{1.16}$$

$M(E)$ can be calculated [54] from the dispersion relation equation (1.7)

$$M(E) = W\frac{2|E|}{\pi\hbar v_F}. \tag{1.17}$$

Equation (1.17) present a linear relation with the energy. From equations (1.14)-(1.17), under the approximation that $-\frac{\partial f}{\partial E} \approx \delta(E - E_F)$ valid for $T \to 0K$, we obtain

$$\sigma = \frac{2e^2}{h}\left(\frac{2E_F}{\pi\hbar v_F}\right)\lambda(E_F). \tag{1.18}$$

In the ballistic regime $\lambda = L$, while for diffusive regime

$$\lambda(E) = \frac{\pi}{2}v_F\tau(E) \tag{1.19}$$

where τ is the momentum relaxation time.

Now, we can introduce the mobility μ defined for bidimensional materials as:

$$\mu = \frac{\sigma}{en} \qquad \left[\frac{V}{cm^2\ s}\right] \tag{1.20}$$

which is valid for both diffusive and ballistic regime. From the definition, the μ is also affected by the scattering process that occurs in graphene at a given temperature [50–52].

In the ballistic regime $\sigma \propto \sqrt{n}$ (Fig. 6) and $\mu \propto 1/\sqrt{n}$. This dependence has been experimentally observed [55]. Experimental value of μ as high as $2 \times 10^5 cm^2 V^{-1} s^{-1}$ for $n < 5 \times 10^9 cm^{-2}$ have been measured on suspended graphene at liquid helium temperature [56–61]. While on SiO_2 substrate, where the transport is diffusive, a value of $\mu \approx 10 \div 15 \times 10^3 cm^2 V^{-1} s^{-1}$ have been measured [58].

In the diffusive regime $\lambda(E)$ and $\tau(E)$ depend on the scattering mechanisms, which are three in the graphene: Coulomb scattering due to charged impurities, defects and adsorbates, and electron-phonon scattering.

Charge impurity scattering is due to the presence of ions on the graphene surface or on the top of the dielectric. Its effects are more relevant at low energies and the relaxation time corresponding to it varies linearly with energy, $\tau(E) \propto E$, [59,61]. From equations (1.20), (1.13), (1.18) and (1.19) we can observe that there is a linear relation between σ and n (Fig. 6), and μ is independent of n. The Coulomb scattering is mainly due to the charge trapping so its effect can be reduced by using dielectric less prone to trap charge such as BN [60]. Another possible solution is to remove the ions by annealing the sample at high temperature [62].

The short range scattering is due to the presence of inhomogeneities in the graphene lattice such as localized defect, vacancies and crack [48,63]. Its potential can be approximated using a delta function. The resulting scattering rate is proportional to the final density state, so $1/\tau\,(E) \propto E$ and it is temperature independent. In this case the conductivity σ does not depend on n and $\mu \propto 1/n$.

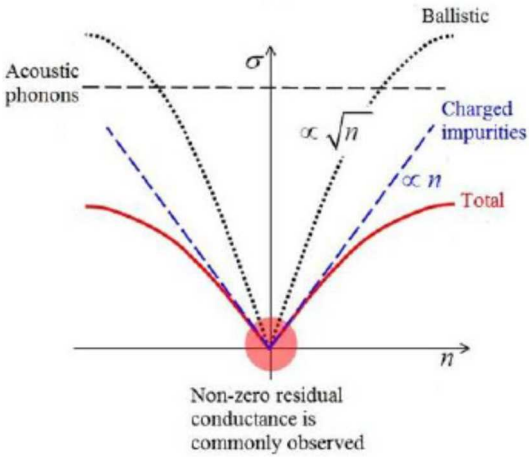


Fig. 6 Conductivity vs carrier density for graphene

The electron-phonon scattering can be considered an intrinsic scattering source and is temperature dependent, so it is present even if there are no imperfections. The scattering of longitudinal acoustic phonons and electrons can be considered quasi-elastic since the phonon energies are negligible respect the electrons Fermi energy [62–64]. Optical phonons can also scatter carriers, especially at temperature above $300K$ and are believed to be responsible

for the decrease in conductivity at high temperature [65]. The total graphene conductivity σ will be equal to

$$\frac{1}{\sigma_{Tot}} = \frac{1}{\sigma_1} + \frac{1}{\sigma_2} + \cdots, \tag{1.21}$$

where σ_i is the conductivity corresponding to a given scattering process.

1.4 Graphene Doping

Graphene can be doped by a chemical approach, using two different methods.

1.4.1 Substitutional doping

This method consists of the introduction of different atoms in the graphene lattice during the fabrication process and offers a good and stable doping.

Typically, acceptor-like boron and donor-like nitrogen can dope graphene as p-type and n-type respectively. The substitution of a graphene atom with a nitrogen one is achieved introducing N-contained precursor gas such as NH_3, CH_3CN, and C_5H_5N, accompanied by the carbon source in the CVD growth process. Similar results can be achieved by post-growth treatments, such as plasma treatment in N-contained gas. While p-doped graphene can be realized using arch discharge with graphite electrode in the presence of $H_2 + B_2H_6$ or using boron stuffed graphite electrodes. N-doped graphene exhibits a lower carrier mobility but larger on/off ratio than that intrinsic graphene [66,67]. Other elements such as phosphorous,[68] silicon[69] and sulfur[70] can also dope the graphene.

1.4.2 Surface doping

Another method for doping graphene has been achieved by adsorbing inorganic or organic molecules on its surface. This method is not the most efficient, it does not disrupt strongly the electronic structure and its effect will weaken or disappear if these molecules desorb from graphene. Substance such as H_2O_2, NO_2, Br_2, I_2 and tetrafluoro-tetracyanoquinodimethane $(F_4 - TNCNQ)$ are strong electron acceptor and can p-dope graphene [71–73]. Also, PMMA residue can p-doped the graphene[74]. While n-doped graphene can be obtained using NH_3, ethanol, and poly(ethylene imine) (PEI) [75,76]. Graphene can be also doped via hydrogenation, fluorination or chlorination with covalent C-H, C-F or C-Cl bond trough plasma reaction or photochemical process [77,78]. Or by the substrate or metal electrode [79–81], Au and Pt cause p-doping, while Al, Ag, and Cu induce n-doping.

1.4.3 Electrical doping

The graphene E_F can be also shifted by the application of a potential through a gate electrode. Graphene field effect devices (GFETs) operate based on this phenomenon to.

1.5 Optical properties

Graphene possesses also very interesting optical properties thanks to its unique band structure. It is able to absorb light on a broad spectrum ranging from ultraviolet and visible to infrared and terahertz (THz) region.

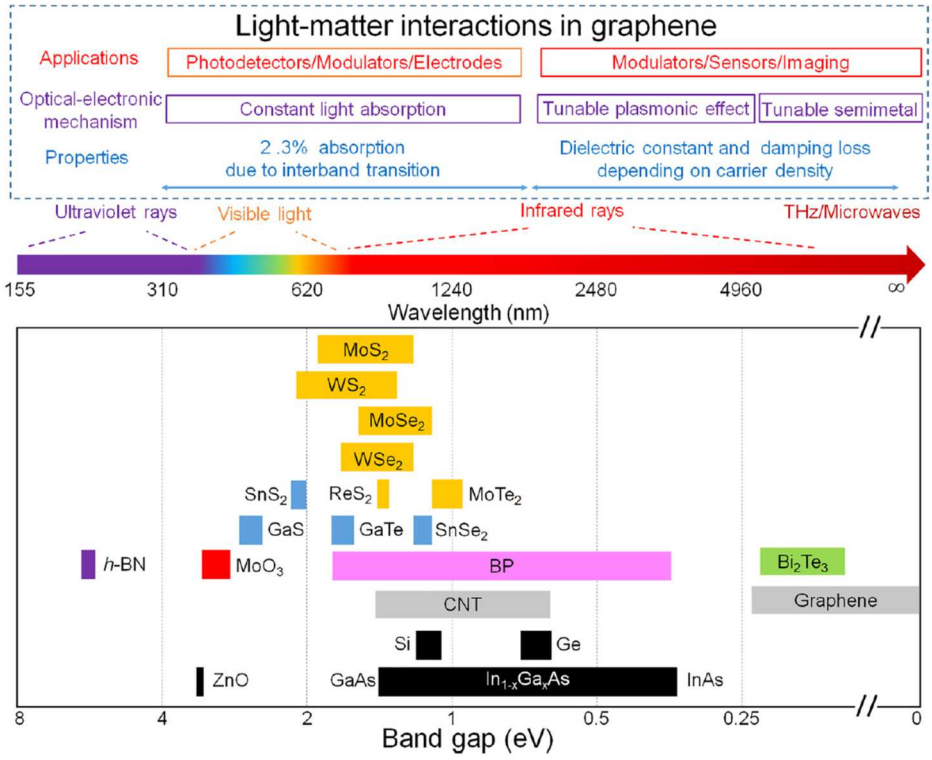


Fig. 7 Electromagnetic spectrum from ultraviolet rays to THz/microwaves and the corresponding light-matter interactions in graphene and the bandgap values for different 2D and conventional semiconductor [18].

When a photon with energy $\hbar\omega$ hit the graphene electron, two photoexcitation mechanisms occur: interband transition and intraband transitions [82,83]. When an electron in the valence band is hit by a photon with energy $\hbar\omega > 2E_F$, it acquires enough energy to jump from the valence to the conduction band leaving behind a hole. This phenomenon is known as interband transition. If the energy $\hbar\omega < 2E_F$, the electron does not possess enough energy to jump and intraband transition occurs (Fig. 7a) .The light-graphene interaction can be described in terms of complex dynamical conductivity $\sigma = \sigma_{inter} + \sigma_{intra}$. Using the random phase approximation (RPA),[83–85] we obtain

$$\sigma = \frac{e^2}{4\hbar}\left[\theta\left(\omega - \frac{2E_F}{\hbar}\right) - \frac{i}{2\pi}\ln\left(\frac{\omega + 2E_F/\hbar}{\omega - 2E_F/\hbar}\right)^2\right] + \frac{ie^2 k_B T}{\pi\hbar(\omega + i\tau^{-1})}\left[\frac{E_F}{k_B T} + 2\ln\left(\exp\left(-\frac{E_F}{k_B T}\right) + 1\right)\right]. \quad (1.22)$$

The first term represents the conductivity due to the interband transition. The step function $\theta(\omega)$ conveys the condition for a photon exciting an electron from the valence band to the conduction band. The second term represents the intraband transition described by the free electron model or Drude model. For the Fermi-Dirac statistic, if $E_F \gg k_B T$, the intraband conductivity becomes:

$$\sigma_{intra} = \frac{ie^2|E_F|}{\pi\hbar(\omega + i\tau^{-1})}. \quad (1.23)$$

Once the conductivity is determinated, the permittivity of graphene can be calculated from $\varepsilon = i\sigma/\omega$, as well the refraction index $n_i = \sqrt{\varepsilon}$. The dynamic conductivity measured in the wavelength from the visible light region to THz region is shown in Fig. 8 b) and c).

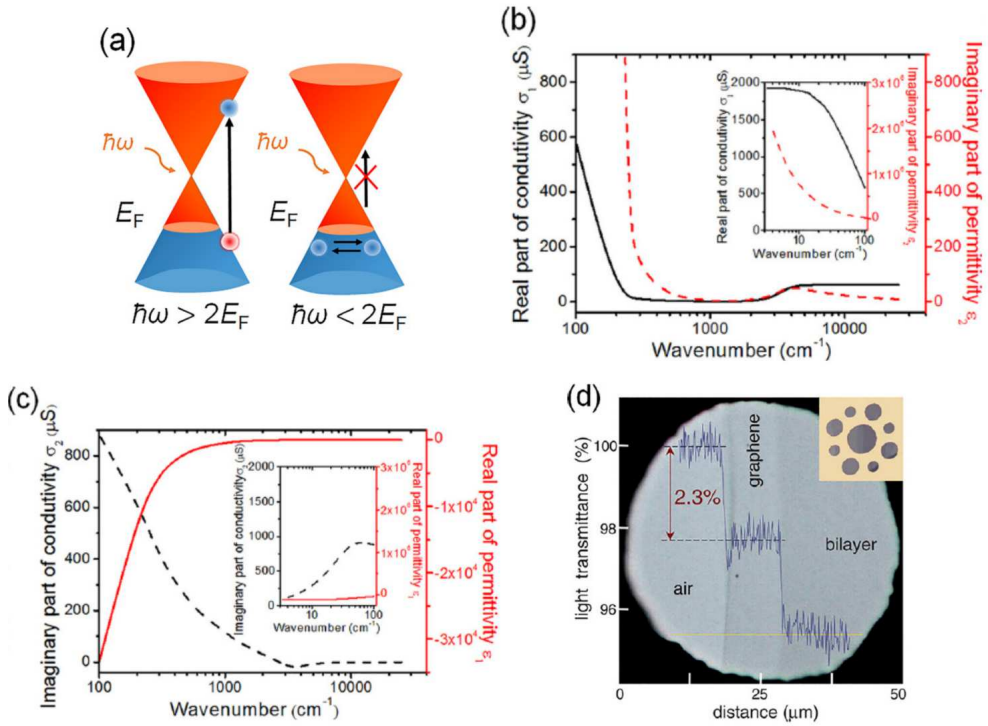


Fig. 8 (a) Interband (left) and intraband (right) transition in graphene. The real part(b) and the imaginary part (c) of conductivity (black line) and corresponding imaginary part (b) and real (c) of permittivity (blue dash line) from visible to far infrared region for graphene; the inset is the THz region. (d) Looking through one-atom-thick crystals. (A) Photograph of a 50-mm aperture partially covered by graphene and its bilayer. The line scan profile shows the intensity of transmitted white light along the yellow line. (Inset) [86]

Let's consider the case the graphene is illuminated by photon with energy $\hbar\omega > 2E_F$ (from visible to near infrared light), the dynamical conductivity (1.22) is dominated by loss (real part) due to the interband transition and the real part of the first term becomes $e^2/4\hbar$. We obtain a constant light absorption of 2.3%, Fig. 8 d). In the lower frequency region, such as infrared and THz region, the dynamical conductivity is dominated by the intraband transition. In this case, the graphene responds to light depend on the scattering rate τ^{-1} and the frequency ω. In the case $\omega > \tau^{-1}$, the imaginary part of the conductivity dominates, and the graphene exhibits a negative permittivity with ohmic losses, and $\varepsilon = i\sigma/\omega$. If $\omega \ll \tau^{-1}$, the real part of conductivity is much larger than the imaginary part. In this case graphene exhibits a metal reflection due to the high conductivity in the THz to microwave region [87,88].

1.6 Graphene Synthesis

Graphene can be fabricated using different methods: 1) micro-mechanical exfoliation of highly ordered pyrolytic graphite, 2) chemical vapour deposition (CVD), 3) epitaxial growth on Silicon Carbide (SiC), and 4) reduction of graphene oxide (GO).

The micro-mechanical exfoliation of highly ordered pyrolytic graphite (HOPG) was first introduced by Prof. Geim and Prof. Novoselov in 2004 [1]. The method is very simple, flakes of HOPG are repeatedly peeled using scotch tape until fading layers of graphite are left on the tape. The flakes are then transferred by pressing the scotch tape onto a substrate, typically Si or SiO_2.

The CVD fabrication method uses a mixture of methane (or any other hydrocarbon) and hydrogen in argon under low pressure and use a metal as a catalyst and substrate to grow graphene [89]. The growth of the graphene takes place at the temperature of $\sim 1000\ °C$. At this temperature, the composition of the carbon containing gas on the metal surface creates a concentration gradient between the surface and the bulk, causing carbon atoms to diffuse into the metal and form a solid solution. Upon cooling, carbon atoms dissolved in the metal at high temperature precipitate out and segregate at the metal surface, forming one or more graphene layer. Metal such as Cu, Ni, Ru, Ir are the most used one. After a thin layer of poly(methyl methacrylate) (PMMA) is spin coated on it.

Graphene layers can be epitaxially formed by heating silicon carbide (SiC) in ultra-high vacuum to temperature between $1000°C$ and $1500°C$ [90,91]. Hexagonal 4H-SiC and 6H-SiC polytypes are commonly employed. The high temperature causes Si to sublimate and leaves behind a carbon rich surface which is graphitic in nature and can be used to form graphene.

The reduction of the GO allows to obtain graphene from raw graphite. This method is cheaper than the other shown before due to the low cost of the material and the chemicals. Further details can be found in [92–94].

All these methods have pros and cons. The micro-mechanical exfoliation method allows to fabricate high-quality graphene, but the films size is tens of micrometres and is not scalable[95]. By reducing the GO is possible to fabricate large quantities of flakes that can be stack together to form larger flakes, but the electrical properties are worse than the flakes obtained from micro-mechanical exfoliation [96]. Graphene epitaxially growth from SiC possesses a good charge mobility and electrical conductivity, but the layer surface is limited by the size of high-quality SiC substrates [97]. The CVD fabrication method can be used to grow large high quality graphene with high electrical conductivity and high charge mobility on transition metal, usually copper [98,99]. The pros of the CVD fabrication methods are the compatibility with the integrated circuit fabrication process [8], the low cost and the efficiency. The cons are the formation of cracks and the presence of chemical residue due to the etching and the transfer process [100,101] which can alter the graphene electronic properties.

1.7 Graphene Wet Transfer Process

Graphene obtained from the scotch tape method can be easily transfer by pressing the scotch tape with the flakes on the substrate. As we explained before this method allow to obtain high-quality graphene but is not possible to control the flakes dimension. The CVD fabrication method has been considered as the best solution to produce large area high-quality graphene layers. The result of this process is a structure composed by the substrate

(in this case we will consider copper foil), a graphene monolayer and the PMMA layer. The PMMA layer has the function to protect and to sustain the graphene layer.

In the following, we will describe a typical wet transfer process using commercial graphene from Graphenea®. Starting from a PMMA/graphene/Cu sample, squares with similar size are cut and place between two Petri plate in order to reduce the wrinkles (Fig. 9 (a)). Cu is etched using a solution of $2 \div 3\ gr$ of ammonium persulfate (APS) and $50\ ml$ of deionized water (DI). The PMMA/graphene/Cu sandwich is placed on the solution with the PMMA on top (Fig. 9 (b)) and it is left rest until the Cu is complete etched.

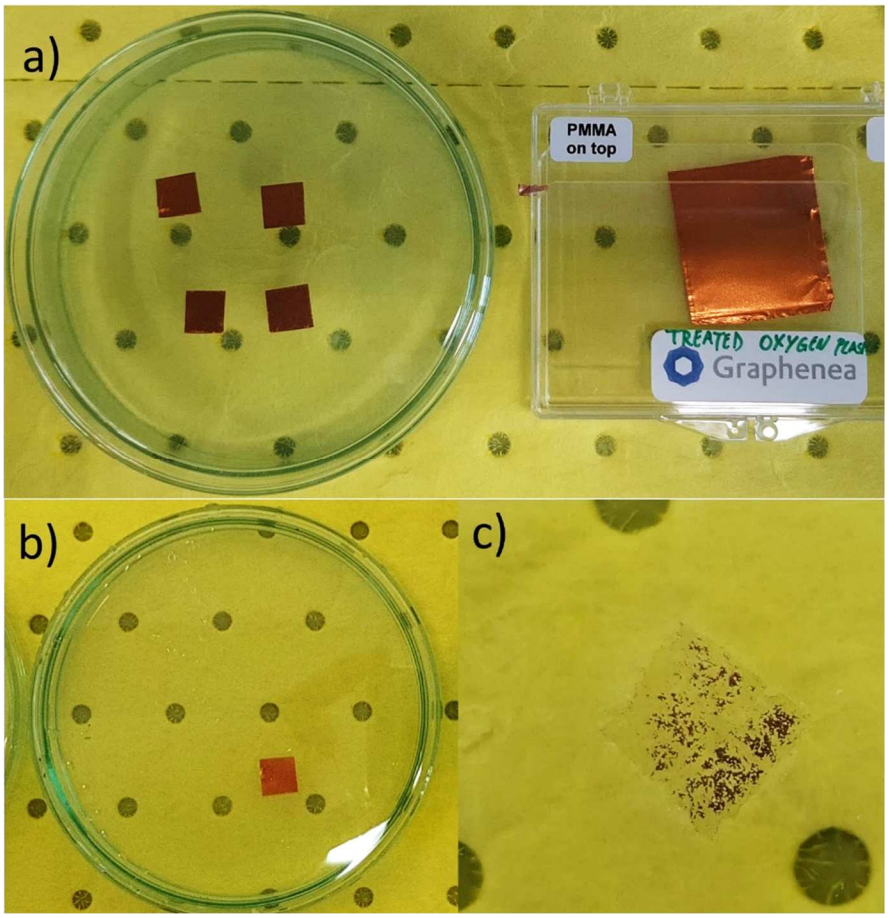


Fig. 9 (a) Commercial Cu/graphene/PMMA stack cuttend in four pieces. (b) Cu/graphene/PMMA stack floating on the APS and DI solution. (c) graphene/PMMA after one hour in the etching solution, trace of the Cu foil are visible.

The PMMA/graphene is fished using a microscope slide, it is put into another Petri plate filled with DI and washed. This step can be repeated many times to ensure the complete removal of Cu traces. At this point the PMMA/graphene is fished using the desired substrate and left to dry (Fig. 10 (a)). When it has dried completely (Fig. 10 (b)), the PMMA top layer is removed with an acetone bath and isopropanol.

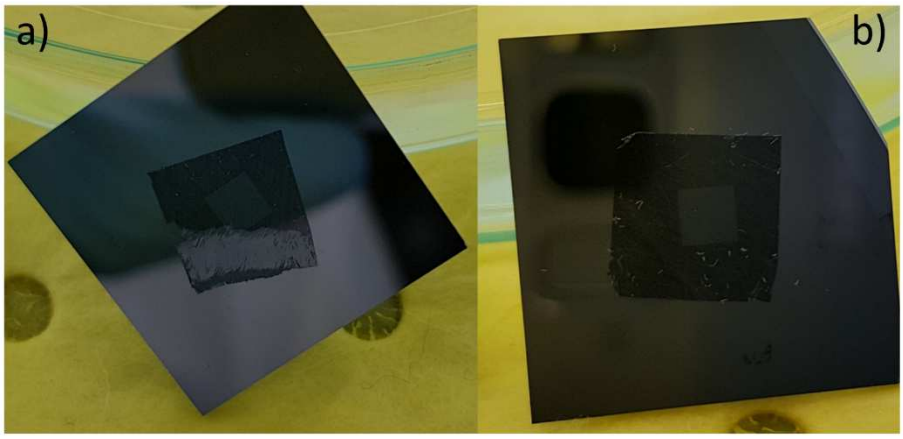


Fig. 10 (a) Graphene/PMMA stack deposited on Si/SiO_2, the substrate is inclined to favour the water evaporation. The water under the graphene tend to accumulate on the bottom. (b) Photo of a dried sample.

2 Schottky Junction

In the previous chapter, we described the graphene structure and its electronic properties. We observed that graphene possesses a bandgap-less structure which make it a semimetal. As we will explain in chapter 3, graphene/silicon heterojunction behaves as a metal/semiconductor Schottky diode. For this reason, we will briefly discuss here the physical phenomena in this type of junction. This chapter content are a sunt of what it is already widely known and described in the reference [102–104].

2.1 Equilibrium in electronic system

All electronic devices communicate through metal/semiconductor contact. The properties of these contacts can vary considerably, and it is necessary to consider several factors in order to understand them. We will start by considering in general the nature of the thermal equilibrium that is established when a metal and a semiconductor are in intimate contact. Application of the equilibrium principles to metals and semiconductors provides a simple theory of ohmic and rectifying behaviour in various metal semiconductor system. This theory does not fully describe the system, we have also to consider effect due to the nature of solid interfaces.

Let us consider the band structure of a metal (m) and a semiconductor (s). When the two system are separate and do not interact with each other, both the systems of electronic states and their Fermi level are independent. Each system has a density of allowed states $N(E)$ per unit energy, part of them are occupied $n(E)$ while the other are empty $v(E)$. These quantities are related by the Fermi-Dirac distribution function:

$$f_{m,s} = \frac{1}{1 + \exp\left(\frac{E - E_{fm,s}}{kT}\right)} \tag{2.1}$$

where $E_{fm,s}$ are the Fermi level of the metal and the semiconductor. The filled state density is obtained from the relation:

$$n_{m,s} = g_{m,s} \times f_{m,s} \tag{2.2}$$

where $g(E)$ is the density of allowed states per unit energy, while the vacant from:

$$v_{m,s} = g_{m,s} \times \left(1 - f_{m,s}\right) \tag{2.3}$$

Let us bring the two system into intimate contact, they begin to interact. The electrons flow from one to the other until the equilibrium is reached and there is no exchange of charge. This does not mean the cession of all process, rather it means that every process and its inverse are occurring at the same rate. Equilibrium can be expressed mathematically by considering that the transfer probability is proportional to the population of the electrons $n(E_x)$ available to transfer at given energy E_x and also proportional to the density of the available states $v(E_x)$ to which the electron can transfer. Therefore, at thermal equilibrium:

$$n_m \times v_s = n_s \times v_m \tag{2.4}$$

at any given energy.

Using equations (2.2) and (2.3) in equation (2.4), we have

$$f_m g_m g_s = f_s g_s g_m \tag{2.5}$$

Equation (2.5) can only be true if $f_m = f_s$ or, by equation (2.1), if $E_{f1} = E_{f2}$. This means any two system are in thermal equilibrium when they have the same Fermi energy.

2.2 Ideal Metal-Semiconductor Junction

Let's consider the band structure of a metal and a n-doped semiconductor which do not interact with each other, Fig. 11. In the metal, the Fermi level is immersed within a continuum of allowed states, while in a semiconductor, under usual circumstance, the density of the states is negligible at the Fermi level.

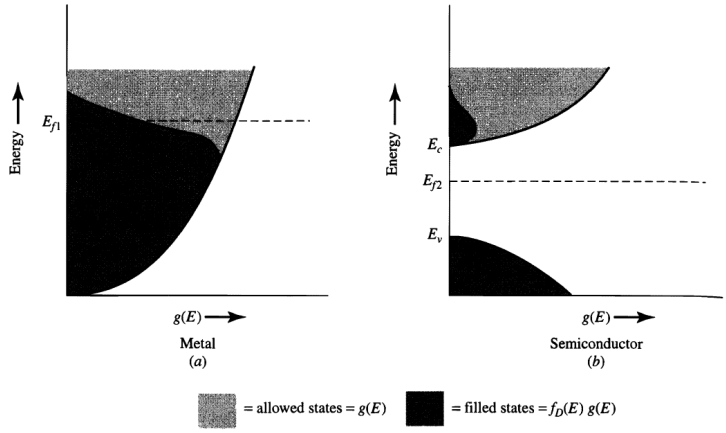


Fig. 11 a) Allowed electronic energy states g(e) in an ideal metal and b) in a semiconductor.

For our discussion we will consider the general schematic view of Fig. 12. E_0 is the energy an electron would have if it were free from any influence of the material and it is called vacuum or free-electron energy. $q\phi$ is the workfunction of the material and it is equal to the difference between E_0 and E_f. E_c and E_v are the conduction and the valence band. The difference of the E_c and E_v is the band gap. The semiconductor Fermi level reside in the bandgap and it can be shift by doping the semiconductor. The difference between the vacuum level and the E_c is the electron affinity $(q\chi)$ and it is a constant of the material.

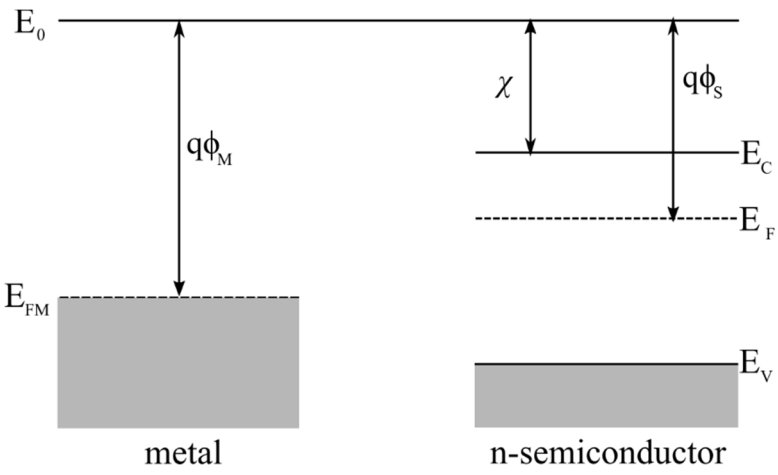


Fig. 12 Energy level of an ideal metal and a n-doped semiconductor.

Let us consider the case the $q\phi_m > q\phi_s$ and the semiconductor is n-doped. When the two system are brought together, they begin to interact with each other as we described before until they reached the thermal equilibrium and the Fermi level is constant for both of them, Fig. 13.

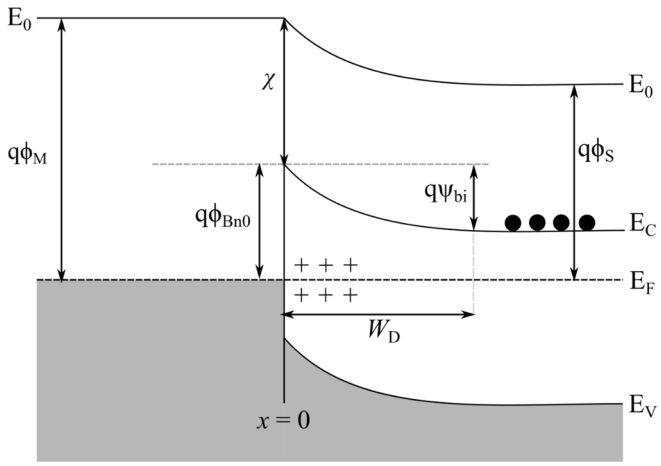


Fig. 13 Idealized equilibrium band diagram for a metal-semiconductor rectifying contact.

Now, we can define the Schottky barrier as the difference of the $q\phi_M$ and the χ

$$q\phi_{Bn0} = q(\phi_M - \chi) \tag{2.6}$$

W_D is the depletion layer and $q\psi_{bi}$ is the built-in potential which we will discuss later. Conversely, in the case the semiconductor is p-doped, the Schottky barrier will be

$$q\phi_{Bp0} = E_g - q(\phi_M - \chi). \tag{2.7}$$

When the junction is formed, electrons flow from the semiconductor to the metal surface leaving behind a region of positive ion. This region is known as depletion layer W_D. This

distribution will form an electric field which prevent further charge exchange. The charge and electric field diagram are plotted in Fig. 14.

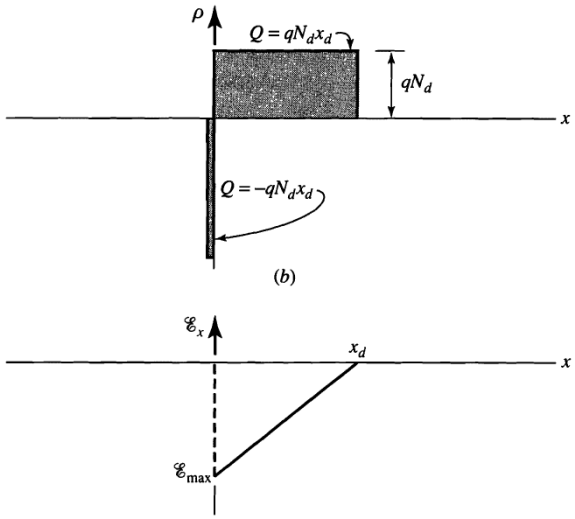


Fig. 14 Charge at idealized metal-semiconductor junction.

Before we determinate the electric field ($\mathcal{E}$) andW_D, let's assume that the charge density $\rho \approx qN_D$, where N_D is the doping concentration, for $x < W_D$ and the $\mathcal{E} \approx 0$ and $\rho \approx 0$ for $x > W_D$. We obtain

$$W_D = \sqrt{\frac{2\varepsilon_S}{qN_D}\left(\psi_{bi} - V - \frac{kT}{q}\right)} \tag{2.8}$$

$$|\mathcal{E}(x)| = \frac{qN_D}{\varepsilon_S}(W_D - x) = \mathcal{E}_m - \frac{qN_D x}{\varepsilon_S} \tag{2.9}$$

$$E_C(x) = q\phi_{B0} - \frac{q^2 N_D}{\varepsilon_S}\left(W_d x - \frac{x^2}{2}\right) \tag{2.10}$$

Where the term kT/q arise from the contribution of the majority of carrier distribution tail and $\mathcal{E}_m$ is maximum electric field strength which occurs at $x = 0$:

$$\mathcal{E}_m = \mathcal{E}(x = 0) = \sqrt{\frac{2qN_D}{\varepsilon_S}\left(\psi_{bi} - V - \frac{kT}{q}\right)} = \frac{2\left[\psi_{bi} - V - \left(\frac{kT}{q}\right)\right]}{W_D}. \tag{2.11}$$

The space charge Q_{SC} per unit of area of the semiconductor and the depletion layer capacitance C_d per unit area are given by

$$Q_{SC} = qN_D W_D = \sqrt{2q\varepsilon_S N_D\left(\psi_{bi} - V - \frac{kT}{q}\right)} \tag{2.12}$$

$$C_D = \frac{\varepsilon_S}{W_D} = \sqrt{\frac{q\varepsilon_S N_D}{2\left[\psi_{bi} - V - \frac{kT}{q}\right]}}. \tag{2.13}$$

Eq.(2.13) can be written in the form

$$\frac{1}{C_D^2} = \frac{2\left[\psi_{bi} - V - \frac{kT}{q}\right]}{q\varepsilon_S N_D} \tag{2.14}$$

or

$$N_D = \frac{2}{q\varepsilon_S}\left(-\frac{1}{d(1/C_D^2)/dV}\right). \tag{2.15}$$

If N_D is constant through the depletion region, a straight line is obtained by plotting $1/C_D^2$ versus the voltage. If N_D is not a constant, the differential capacitance method can be used to determinate the doping profile from eq.(2.15).

2.3 Interface states

In the previous section, we defined the Schottky barrier as the difference between the metal work function and the electron affinity, but we did not consider the effect induced by the interface states.

A detailed energy band diagram of a metal and a n-doped semiconductor is showed in Fig. 15. As we can see there are different energy level and interface trap which can affect the junction. The first one we are going to consider is the energy level $q\phi_0$ above the E_V at the surface. It is called the neutral level and above it the states are of acceptor type (neutral when empty and negative when occupied) and below the states are of donor type (neutral when full of electrons, positively charged when empty). The presence of these traps can affect the Schottky barrier height.

Let's consider the case of a semiconductor with acceptor interface trap whose density is D_{it} states/cm^2·eV and let's suppose it is constant over the energy range from $q\phi_0 + E_V$ to the Fermi level. The interface-trap charge density on the semiconductor Q_{SS} is therefore negative and is given by

$$Q_{SS} = -qD_{it}\left(E_g - q\phi_0 - q\phi_{Bn0}\right) \qquad \frac{C}{cm^2}. \tag{2.16}$$

The space charge that forms in the depletion layer of the semiconductor at thermal equilibrium is given as

$$Q_{SC} = qN_D W_D = \sqrt{2q\varepsilon_S N_D\left(\phi_{Bn0} - \phi_n - \frac{kT}{q}\right)}. \tag{2.17}$$

The sum of (2.16) and (2.17) is equal to the total of the surface charge density on the semiconductor surface. In the absence of any space-charge effects in the interfacial layer, an

exactly equal and opposite charge, Q_M (C/cm^2), develops on the metal surface. For thin interfacial layers such space-charge effects are negligible and Q_M can be written as

$$Q_M = -(Q_{SS} + Q_{SC}) \tag{2.18}$$

The potential Δ across the interfacial layer can be obtained by applying the Gauss' law:

$$\Delta = -\frac{\delta Q_M}{\varepsilon_i} \tag{2.19}$$

where ε_i is the permittivity of the interfacial layer and δ is the thickness. The potential Δ can be also obtained by considering the potentials:

$$\Delta = \phi_m - (\chi + \phi_{Bn0}) \tag{2.20}$$

The potential Δ can be exploited to determinate the relation between the charge densities Q_{SS} and Q_{SC} and the energy-band diagram:

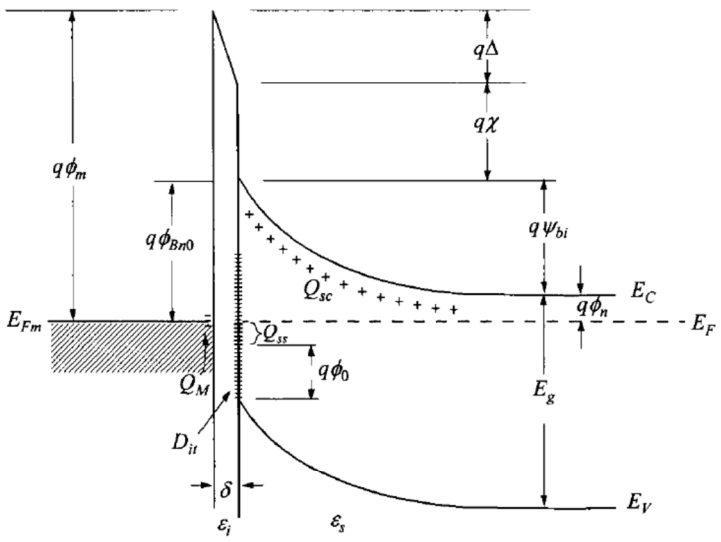
$$\begin{aligned} \phi_m - \chi - \phi_{Bn} \\ = \sqrt{\frac{2q\varepsilon_S N_D \delta^2}{\varepsilon_i^2}\left(\phi_{Bn} - \phi_n - \frac{kt}{q}\right)} \\ - \frac{qD_{it}\delta}{\varepsilon_i}\left(E_g - q\phi_0 - q\phi_{Bn}\right). \end{aligned} \tag{2.21}$$

Let's introduce the quantities

$$c_1 \equiv \frac{2q\varepsilon_S N_D \delta^2}{\varepsilon_i^2} \tag{2.22}$$

$$c_2 \equiv \frac{\varepsilon_i}{\varepsilon_i + q^2 \delta D_{it}} \tag{2.23}$$

which contain all the interfacial properties. c_1 can be calculate from equation (2.22) if values of δ and ε_i are estimated.



ϕ_m = Work function of metal
ϕ_{Bn0} = Barrier height (without image-force lowering)
ϕ_0 = Neutral level (above E_V) of interface states
Δ = Potential across interfacial layer
χ = Electron affinity of semiconductor
ψ_{bi} = Built-in potential
δ = Thickness of interfacial layer
Q_{sc} = Space-charge density in semiconductor
Q_{ss} = Interface-trap charge
Q_M = Surface-charge density on metal
D_{it} = Interface-trap density
ε_i = Permittivity of interfacial layer (vacuum)
ε_s = Permittivity of semiconductor

Fig. 15 Detailed energy band diagram of a metal and n-doped semiconductor with an interfacial layer of the order of atomic distance.

There are two limiting cases which can be obtained directly equation(2.21):

1. When $D_{it} \to \infty$, then $c_2 \to 0$ and

$$q\phi_{Bn0} = E_g - q\phi_0 \tag{2.24}$$

The Fermi level is pinned by the surface states at the value $q\phi_0$ above the valence band. The barrier height is independent of the metal workfunction and is determinated entirely by the surface properties of the semiconductor.

2. When $D_{it} \to 0$, and $c_2 \to 1$ and

$$q\phi_{Bn0} = q(\phi_m - \chi) \tag{2.25}$$

which is the definition of the Schottky barrier when the surface state effects are neglected.

2.4 Image force lowering

Let us consider a metal and n-doped semiconductor junction. As described before, at thermal equilibrium, negative charges will accumulate on the metal surface, while positive charge

will distribute in the semiconductor depletion layer. The force of attraction between the electron and the induced positive charge is equivalent to the force that would exist between the electron and an equal positive charge at $-x$. We will refer to the positive charge as the image charge. The force between the charge and the image charge, known as image force, is

$$F = -\frac{q^2}{4\pi\varepsilon_S(2x)^2} = -\frac{q^2}{16\pi\varepsilon_S x^2} \tag{2.26}$$

The work done to an electron in the course of its transfer from infinity to the point x is given by

$$E(x) = \int_{\infty}^{x} F dx = -\frac{q^2}{16\pi\varepsilon_S x}. \tag{2.27}$$

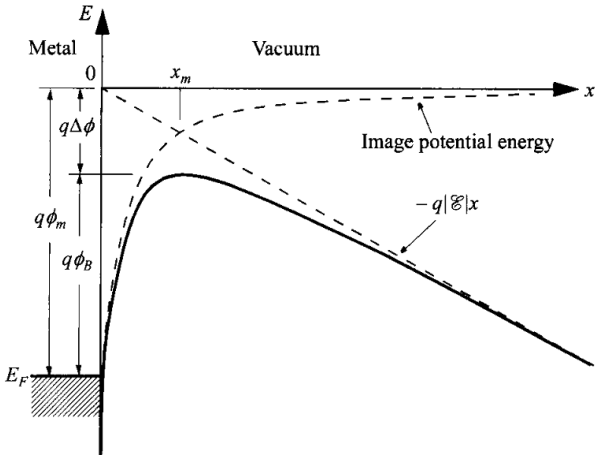


Fig. 16 Energy band diagram of the metal-semiconductor junction considering the Schottky barrier lowering effect.

When an external electric field $\mathcal{E}$ is applied, the electron potential energy (E_{PE}) is

$$E_{PE} = -\frac{q^2}{16\pi\varepsilon_S x} - q\mathcal{E}x. \tag{2.28}$$

The E_{PE} affects the Schottky barrier height reducing it of a quantity $\Delta\phi$ in the point where it is maximum x_m, Fig. 16. x_m and $\Delta\phi$ are given by the conditions $d(E_{PE})/dx$:

$$x_m = \sqrt{\frac{q}{16\pi\varepsilon_S|\mathcal{E}|}}. \tag{2.29}$$

$$\Delta\phi = \sqrt{\frac{q|\mathcal{E}|}{4\pi\varepsilon_S}} = 2|\mathcal{E}|x_m. \tag{2.30}$$

In the Schottky diode, the electric field is not constant with the distance, and the maximum value at the surface based on the depletion approximation can be used,

$$\mathcal{E}_m = \sqrt{\frac{2qN_D|\psi_S|}{\varepsilon_S}}, \tag{2.31}$$

ψ_S is the surface potential:

$$\psi_S = \phi_{Bn0} - \phi_n + V_R. \tag{2.32}$$

where V_R is the reverse bias. Substituting (2.31) in (2.30) we obtain

$$\Delta\phi = \sqrt{\frac{q\mathcal{E}_m}{4\pi\varepsilon_S}} = \left[\frac{q^3 N_D|\psi_S|}{8\pi^2\varepsilon_S^3}\right]^{\frac{1}{4}} \tag{2.33}$$

So, the application of a bias can reduce (reverse bias) or increase (forward bias) the Schottky barrier, Fig. 17, but its effect are related to the doping concentration N_D. The higher the N_D, greater will be the lowering Schottky barrier effect.

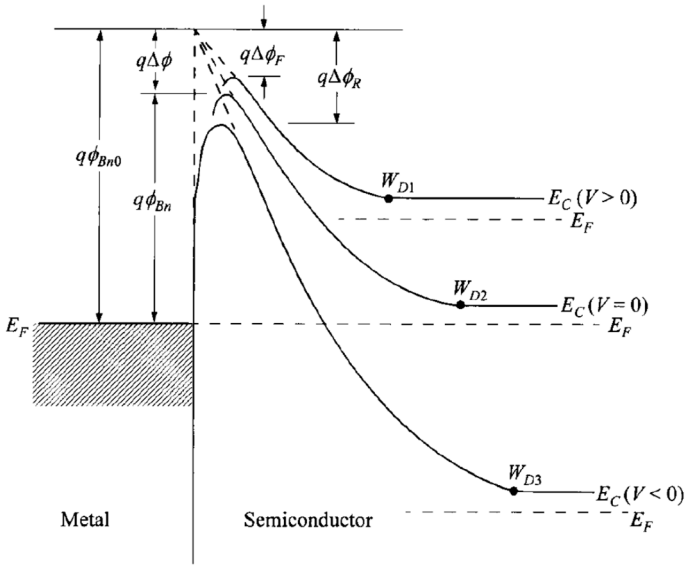


Fig. 17 Energy band diagram of the metal-semiconductor junction at different bias.

2.5 Current voltage characteristic

The current transport in the Schottky diode is mainly due to majority carriers, that is electron for the n-type and holes for the p-type. There are five current transport processes which happen in a metal/semiconductor junction: (1) emission of the electrons from the semiconductor over the potential barrier into the metal, which is the dominant one for moderately doped semiconductor ($N_D < 10^{17} cm^{-3}$), (2) quantum-mechanical tunneling of the electron trough the barrier (heavy doped semiconductor), (3) recombination in the space-charge region (which is similar the one happening in the p-n junction), (4) diffusion of the electrons in the depletion region, and (5) holes injected from the metal that diffuse into the semiconductor.

In this work we will only focus on the thermionic emission model and tunneling current.

2.5.1 Thermionic Emission Current

The thermionic emission theory is derived from the assumption that the barrier height $q\phi_{Bn} \gg kT$, the thermal equilibrium is established at the junction and the current due to the exchange of charges from the semiconductor to the metal is balanced by the one from the metal to the semiconductor. These currents are proportional to the density of electrons at the boundary. At equilibrium, the density n is

$$n = \int_0^\infty f(E)g(E)dE \tag{2.34}$$

where $g(E)$ is the density of allowed states per volume and energy in the semiconductor, and $f(E)$ is the Fermi-Dirac distributions we introduced before. In the semiconductor

$$g(E) = \frac{4\pi}{h^3}(2m_e^*)^{\frac{3}{2}}\sqrt{E - E_C} \quad for\ E > E_C \tag{2.35}$$

where h is the Planck constant and m_e^* is the electron effective mass. The current density from the metal to the semiconductor $J_{M\to S}$ is given by the concentration of electrons with energies enough to overcome the potential barrier and traversing in the x-direction

$$J_{M\to S} = \int_{E_{Fn}+q\phi_{Bn}}^\infty qv_x dn \tag{2.36}$$

From equations (2.34) and (2.35),

$$dn = g(E)F(E)dE \approx \frac{4\pi(2m_e^*)^{\frac{3}{2}}}{h^3}\sqrt{E - E_C}\exp\left(-\frac{E - E_C + q\phi_n}{kT}\right)dE \tag{2.37}$$

Assuming that the electron energy in the conduction band is kinetic energy

$$E - E_C = \frac{1}{2}m_e^* v^2 \tag{2.38}$$

$$dE = m_e^* v dv \tag{2.39}$$

$$\sqrt{E - E_C} = v\sqrt{\frac{m_e^*}{2}}. \tag{2.40}$$

By substituting in equation (2.37), we obtain

$$dn \approx 2\left(\frac{m_e^*}{h}\right)^3 \exp\left(-\frac{q\phi_n}{kT}\right)\exp\left(-\frac{m_e^* v^2}{2kT}\right)(4\pi v^2 dv). \tag{2.41}$$

where

$$v^2 = v_x + v_y + v_z. \tag{2.42}$$

Equation (2.41) is the number of electrons per unit volume that have velocities between v and $v + dv$, distributed over all directions. Since we are considering only the electrons which moves in x-direction, from equation (2.36), we obtain

$$J_{M\to S} = \left(\frac{4\pi q m_e^* k^2}{h^3}\right) T^2 \exp\left(-\frac{q\phi_n}{kT}\right) \exp\left(-\frac{m_e^* v_{0x}^2}{2kT}\right). \tag{2.43}$$

v_{0x} is the minimum velocity required to surmount the barrier and is

$$\frac{1}{2} m_e^* v_{0x}^2 = q(\psi_{bi} - V). \tag{2.44}$$

Substituting in equation (2.43)

$$\begin{aligned} J_{M\to S} &= \left(\frac{4\pi q m_e^* k^2}{h^3}\right) T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \exp\left(\frac{qV}{kT}\right) \\ &= A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \exp\left(\frac{qV}{kT}\right), \end{aligned} \tag{2.45}$$

and

$$A^* = \frac{4\pi q m_e^* k^2}{h^3} \tag{2.46}$$

is the Richardson constant for thermionic emission, neglecting the effects of optical-phonon scattering and quantum mechanical reflection. For free electrons ($m_e^* = m_0$) the Richardson constant is $120\ A/cm^2K^2$. Although the Richardson constant depends on the material properties of the semiconductor, it has been demonstrated that the metal, the presence of inhomogeneity in the Schottky barrier, interfacial layer, quantum mechanical reflections and tunnel of carrier, can cause some variation.

According to (2.45), $J_{S\to M}$ depends on the Schottky barrier height, but not to its shape and it strongly depends on the applied voltage bias, being exponentially increased (decreased) by positive (negative) bias. The total density current through the junction is equal to the sum of the density current from the metal to the semiconductor ($J_{M\to S}$) and the density current from the semiconductor to the metal ($J_{S\to M}$). Since the metal workfunction is bias independent, J_{MS} can be determinate by applying the equilibrium condition ($V = 0\ V$):

$$J_{M\to S} + J_{S\to M} = 0 \tag{2.47}$$

$$J_{M\to S} = -J_{S\to M} = A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right). \tag{2.48}$$

The total current density is then

$$J_n = \left[A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right)\right]\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

$$= J_0 \left[\exp\left(\frac{qV}{kT}\right) - 1 \right], \tag{2.49}$$

where

$$J_0 \equiv A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \tag{2.50}$$

is the saturation density current.

2.5.2 Tunneling Current

In the case of high doped semiconductor and/or for operation at low temperatures, the tunneling current may become significant. The tunneling current from the semiconductor to the metal $J_{S\to M}$ is proportional to the quantum transmission coefficient (tunneling probability) multiplied by the occupation probability in the semiconductor and the unoccupied probability in the metal, that is,

$$J_{S\to M} = \frac{A^* T^2}{kT} \int_{E_{FM}}^{q\phi_{Bn}} F_S T(E)(1 - F_M) dE. \tag{2.51}$$

F_S and F_M are the Fermi-Dirac distribution functions for the semiconductor and the metal respectively, and $T(E)$ is the tunneling probability which depends on the width of the barrier at a particular energy. The density current from the metal to the semiconductor is similar to (2.51) and flow from the opposite direction.

The tunneling current contribution induced a deviation of the ideal thermionic emission I-V. In forward, the rise of the current can be better described by inserting a phenomenological parameter η in the exponential in equation (2.49)

$$J = J_0 \left[\exp\left(\frac{qV}{\eta kT}\right) - 1 \right] \tag{2.52}$$

η is known as ideality factor. In Fig. 18 are plotted the current density J_0 and η for Au-Si diode as a function of doping concentration. J_0 is constant for low doping, but starts to increase rapidly when $N_D > 10^{17} cm^{-3}$. η is very close to unity at low doping and high temperature, but it begins to increase at higher doping concentration and lower temperature.

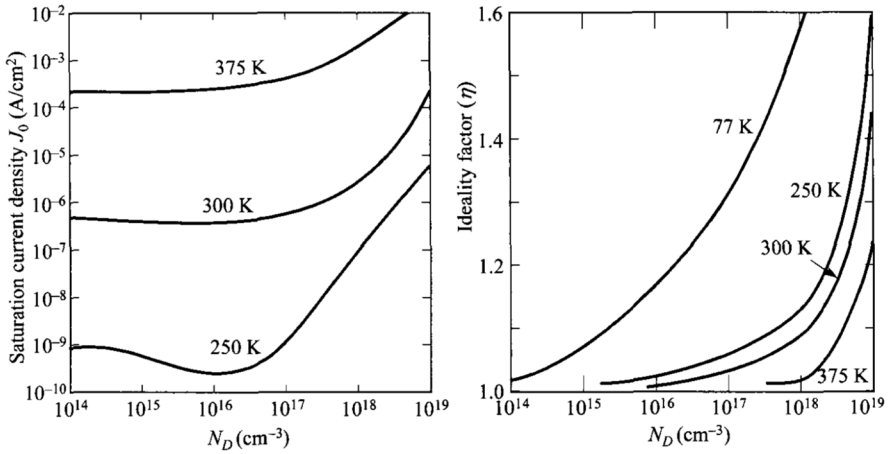


Fig. 18 Density saturation current J_0 and ideality factor η as function of the doping concentration.

In Fig. 19 is shown the ratio of the tunneling current to the thermionic of an Au-Si barrier diode. For doping concentration $N_D \leq 10^{17} cm^{-3}$ and $T > 300K$, the ratio is much less than unity and the tunneling current component can be neglected. While at higher doping level and lower temperature, the ratio can become much larger than unity, indicating that the tunneling current becomes dominant.

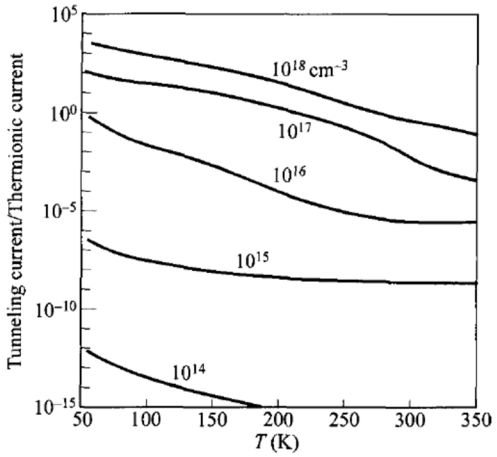


Fig. 19 Ratio of the tunneling current to the thermionic current in Au-Si Schottky junction.

2.5.3 Effect of the bias dependence of Schottky barrier

In the previous paragraphs, we determinated the thermionic density current equation and we introduced the ideality factor to consider the contribution from the tunneling density current. The ideality factor can be also used to consider other phenomena such as the lowering barrier effect induced by the applied bias.

Let us consider the general case of either n-type or p-type semiconductor, and suppose that ϕ_B depends linearly on the applied bias V, which is true for small value of V, so that we can write

$$\phi_B = \phi_{B0} + \beta V \tag{2.53}$$

β is positive because ϕ_B increases with increasing forward bias. We can rewrite (2.49) as

$$J = A^* T^2 \exp\left[-\frac{q(\phi_{B0} + \beta V)}{kT}\right]\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

$$= J_0 \exp\left(-\frac{q\beta V}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{2.54}$$

Equation (2.54), can be rewritten as

$$J = J_0 \exp\left(\frac{qV}{\eta k}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \tag{2.55}$$

where

$$\frac{1}{\eta} = 1 - \beta = 1 - \frac{\partial \phi_B}{\partial V} \tag{2.56}$$

2.5.4 MIS Tunnel Diode

Until now we have considered ideal homogeneous metal semiconductor junction. In reality, a thin layer of oxide is usually introduced before the metal deposition. This interfacial layer thickness lies in the rage of $1 - 3\ nm$. The presence of an oxide layer (1) reduces the current, (2) forms a lower barrier height and (3) higher ideality factor η.

The density current equation (2.52) can be rewritten by introducing a tunneling attenuation factor $\exp(-\sqrt{\chi} \cdot \delta)$ where χ (in eV) is the effective barrier, δ (in Å) is the thickness of the interfacial layer and $C = [2(2m_e^*/\hbar^2)]^{1/2} \approx 1.01\ eV^{-1/2}Å^{-1/2}$:

$$J = A^* T^2 \exp\left(-\sqrt{\chi} \cdot \delta \cdot C\right) \exp\left(-\frac{q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right] \tag{2.57}$$

C is usually omitted

$$J = A^* T^2 \exp\left(-\sqrt{\chi} \cdot \delta\right) \exp\left(-\frac{q\phi_B}{kT}\right)\left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right] \tag{2.58}$$

The ideality factor η is increased to

$$\eta = 1 + \left(\frac{\delta}{\varepsilon_i}\right)\frac{\left(\frac{\varepsilon_S}{W_D}\right) + qD_{its}}{1 + \left(\frac{\delta}{\varepsilon_i}\right) qD_{itm}} \tag{2.59}$$

where D_{its} and D_{itm} are interface traps in equilibrium with the semiconductor and metal, respectively. When the oxide layer is less than $3\ nm$, the interface traps are in equilibrium with the metal, while for thicker oxides the traps tend to be in equilibrium with the semiconductor.

In conclusion the interfacial layer reduces the majority carrier thermionic emission current, but it doesn't affect the minority carrier current, which is from diffusion, and raises the

minority injection efficiency. This phenomenon is exploited to improve the Schottky solar cell open-circuit voltage.

2.6 Measurement of the Schottky parameters

Determining the Schottky diode parameters, which must be considered in practical application, plays an important role in the designing and manufacturing process.

We previously described the forward bias J-V characteristic for ideal diode, equation (2.52) , in this case we will consider the real case and thus the potential drop due to the series resistance (R_S). Let's rewrite equation (2.52) by taking into account also the surface junction A,

$$J \cdot A \equiv I = I_0 \left[\exp\left(\frac{q(V - IR_S)}{\eta kT} \right) - 1 \right] \tag{2.60}$$

where I_0 is the saturation current defined as

$$I_0 = AA^* T^2 \exp\left(-\frac{q\phi_B}{kT} \right). \tag{2.61}$$

$q\phi_B$ can be easily extracted from the reverse saturation current (2.61) when all variable are known. Eq. (2.61) allows to determinate the $q\phi_B$ when all other parameters are known, but it does not give any information about the quality of the junction (η).

Let's consider the range where the series resistance R_S can be neglected ($V \gg IR_S$), equation (2.60) can be rewritten in the form of

$$\ln(I) = \ln(I_0) + \frac{qV}{\eta kT}. \tag{2.62}$$

By doing so, we obtain a linear relation between the diode logarithmic current and the voltage. The reverse saturation current and the ideality factor can be extracted from the linear fit intercept and slope, respectively. Once the I_0 is obtained, the $q\phi_B$ can be extrapolated from (2.61). This analysis is quite simple and allows to extrapolate the Schottky barrier easily if A^* is known. Although A^* values are reported for every semiconductor [102], the presence of an insulator layer in the junction (see paragraph 2.5.4) or inhomogeneity can reduce it making the $q\phi_B$ obtained inaccurate. By rewriting equation (2.61) in the form of

$$\ln \frac{I_0}{T^2} = \ln(AA^*) - \frac{q\phi_B}{kT}. \tag{2.63}$$

we obtain the Arrhenius plot where the Richardson constant and the Schottky barrier can be extrapolated from the its intercept and slope, respectively. I_0 are the reverse saturation currents obtained from the linear fit of equation (2.62) performed on the ln(I)-V measured at different temperatures T.

We have to determinate now the series resistance.

Unfortunately, the determination of the R_S is not a simple task, equation (2.60) is in fact, a transcendental equation. Therefore, the R_S cannot be determinated analytically but it can be approximated. Different methods were proposed, most of them use some auxiliary function, such as the derivative or the integration of the current with respect to the voltage and several I-V measurements at different temperatures [105]. We will not focus on all of them, but the one we used in this work, i.e. the Cheung and Cheung method and the Lien-Norde method.

2.6.1 The Cheung and Cheung method

Another way to determinate the Schottky diode parameters was proposed by S.K. Cheung and N. W. Cheung in 1986 [106]. The Cheung and Cheung (C.C.) method allows the determination of the Schottky barrier, the ideality factor and the series resistance value at different temperatures.

Let's consider equation (2.60) and rewrite it in the form

$$V = R_S I + \eta\phi_B + \left(\frac{\eta}{kT}\right)\ln\left(\frac{I}{AA^*T^2}\right), \tag{2.64}$$

Differentiating equation (2.64) with respect to $\ln I$ we obtain

$$\frac{d(V)}{d(\ln I)} = R_S I + \frac{\eta}{kT}, \tag{2.65}$$

the R_S and the η can be determinated from the slope and the intercept respectively. The determination of the Schottky barrier can be done by defining the function $H(I)$ as

$$H(I) \equiv V - \left(\frac{\eta}{kT}\right)\ln\left(\frac{I}{AA^*T^2}\right), \tag{2.66}$$

From equation (2.64) we obtain

$$H(I) = R_S I + \eta\phi_B \tag{2.67}$$

Once the ideality factor is determined, the right side of Equation (2.66) can be computed. According to Equation (2.67), the $H(I)$ vs. I plot is a straight line whose slope and intercept are the R_S and the product $\eta\phi_B$, respectively. The R_S obtained from equation (2.67) can be used to check the consistency of this approach.

This method allows to determinate the R_S, the η, and the ϕ_B value at different temperature which is of great help to better understand how the Schottky parameters vary from low to high temperatures.

2.6.2 Lien-Norde method

The presence of a series resistance R_S affect the forward current by reducing the interval where the I-V plot is linear. Furthermore, since one is forced to use a range where the bias V is small, recombination current in the diode may be a significant part of the total current making the extrapolated I_0 value still more unreliable.

The Lien-Norde method allow to determinate the Schottky diode parameters using the ideality factor η determinated from the T.E. model and the function $F(V)$ defined as [107,108]

$$F(V) = \frac{V}{\gamma} - \frac{1}{kT}\ln\left(\frac{I(V)}{AA^*T^2}\right). \tag{2.68}$$

where γ is an arbitrary constant greater than the ideality factor. The ϕ_B and the R_S can be determinated as

$$q\phi_B = F(V_{min}) + \frac{\gamma - \eta}{\eta}\left(\frac{V_{min}}{\gamma} - \frac{kT}{q}\right) \tag{2.69}$$

$$R_S = \frac{(\gamma - \eta)kT}{qI_{min}} \tag{2.70}$$

where $F(V_{min})$ and V_{min} are the coordinates of the minimum point in the plot $F(V)$ vs V and I_{min} is the current value at the voltage V_{min}. The accuracy of this method is strictly related to the independence from the parameter γ.

2.6.3 Pros and cons of the methods

All the method listed before cannot be used as stand alone. Some of them can be used to determinate some parameters while other cannot. An example is the Richardson constant A^*. When A^* is unknown it cannot be determinated using the C.C. method and the Norde method, but it can only be determinated from the thermionic emission model. In the same way, R_S cannot be determinated from the thermionic emission model but it can be determinated from the C.C. and Norde method.

2.7 Capacitance-Voltage measurement

The Schottky barrier can be determinate from the I-V characteristic using different method, but it can also determinate from the C-V characteristic. When a small AC voltage is applied upon a DC bias, incremental charges of one sign are induced on the metal surface and charges of the opposite sign in the semiconductor. From equation (2.14) we obtain a linear plot of $1/C^2$ vs V. The intercept plot gives the built-in potential ψ_{bi} from which the barrier height can be determinate:

$$\phi_B = \psi_{bi} + \phi_n + \frac{kT}{q} - \Delta\phi \tag{2.71}$$

From the slope the carrier density can also be determinate (2.15) and it can be used to calculate ϕ_n.

3 Graphene/Silicon Junction

3.1 Modelling of Graphene/Silicon Junction

A theory able to fully describe the graphene/Silicon junction does not exist to-date, although few phenomenological models, explaining experiment features, have been proposed.

S. Tongay et al. tried first to propose a simple modification of the thermionic emission theory to include the bias dependence of the E_F and explain the bias driven-increase of the reverse saturation current [46]. In a metal/semiconductor junction the metal Fermi level stays constant upon the application of a bias because of the high density of states of the metal. When the metal is replaced with graphene, there is an exchange of charges between the $2D$ graphene and a $3D$ silicon.

Let's consider the band structure of the junction formed by a graphene and a n-doped silicon substrate (Fig. 20 (a)). Let assume the graphene Fermi level (E_F) is a t Dirac point and it is aligned with silicon Fermi level (E_{FS}). The Schottky barrier Φ_B will be

$$\Phi_B = \Phi_g - \chi \tag{3.1}$$

where Φ_g is the graphene workfunction and χ is the silicon electron affinity.

Let us suppose the silicon is grounded, and a bias is applied on the graphene. In forward bias, the graphene Fermi level has to shift down to accept the negative charges mirroring the positive on in the depletion layer (Fig. 20 (b)). The effect is small since a low bias is usually applied in forward. Because of that, the Schottky barrier will be a little higher than the equilibrium. In reverse bias (Fig. 20 (c)), the depletion layer increase substantially and so does the negative charges in graphene shifting the Fermi level up. The Schottky barrier will be lower than the equilibrium.

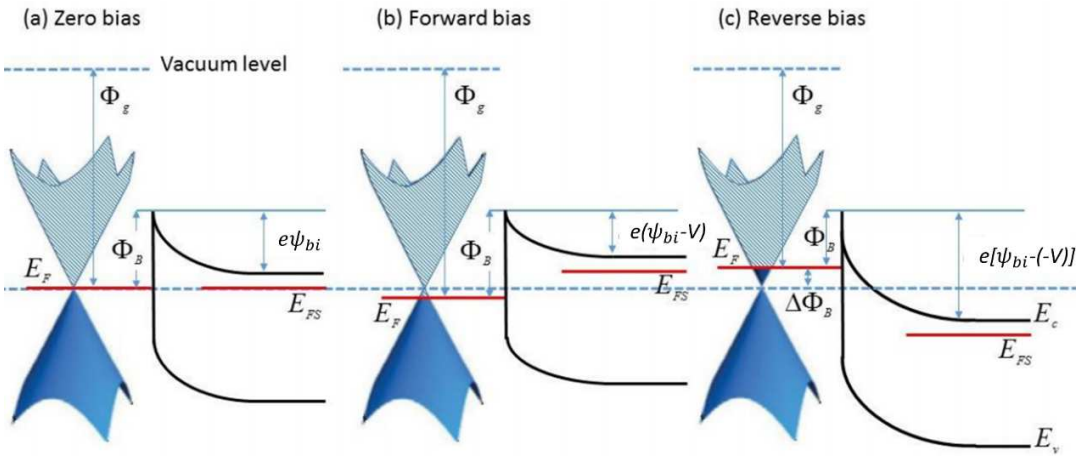


Fig. 20 (a) Band structure of the Gr/Si junction at thermal equilibrium and at 0 V,(b) in forward bias and (c) in reverse bias.

The graphene Fermi level variation due to the bias can be easily included in the thermionic emission model, we introduced before for the Schottky diode, by replacing the constant Schottky barrier with a bias dependent one.

Let's suppose the band alignment hold at zero bias, the graphene carrier density per unit area (n_i) induced by a bias (V) can be expressed by assuming that it is opposite to the density of the positive ion in the depletion layer. From equation (1.12), n_{in} is

$$\begin{aligned} n_{in}(V) &= -\Delta n_{depl} \\ &= -\left(\sqrt{\frac{2\varepsilon_S N_D \left(\psi_{bi} - V - \frac{kT}{e}\right)}{e}} - \sqrt{\frac{2\varepsilon_S N_D \left(\psi_{bi} - \frac{kT}{e}\right)}{e}} \right) \end{aligned} \tag{3.2}$$

When $V > 0$, n_{in} is positive and graphene is p-doped; in reverse bias $(V < 0)$ and $n_{in} < 0$, graphene is n-doped. From equation (1.14)

$$\Delta E_F(V) = \mp \frac{h}{2\sqrt{\pi}} v_F \sqrt{|n_{in}(V)|} \tag{3.3}$$

where the $\mp$ signs corresponds to the down/up shift of E_F in forward or reverse bias, respectively. In the case the graphene already possesses a doping with density n_0, the zero Fermi level will be initially shifted respect the Dirac point by an amount given by equation (3.3) with n_{in} replaced by n_0.

In the case of the application of a bias, the total carrier density per area in graphene is

$$n_g = n_0 + n_{in}(V) = -\sqrt{\frac{2\varepsilon_S N_D \left(\psi_{bi} - V - \frac{kT}{e}\right)}{e}} \tag{3.4}$$

where $n_{in}(V)$ is the bias induced contribution to carriers. If we consider an ideal junction and neglect possible interface states n_{in} results in a variation of the Fermi level which can be expressed as from equation (1.14)

$$\begin{aligned} \Delta E_F(V) &= \frac{h}{2\sqrt{\pi}} v_F \left(\sqrt{|n_g(V)|} - \sqrt{|n_0|} \right) \\ &= \frac{h}{2\sqrt{\pi}} v_F \left(\sqrt{|n_0 + n_{in}(V)|} - \sqrt{|n_0|} \right) \end{aligned} \tag{3.5}$$

At zero bias $\Delta E_F = 0$, when $n_g = n_0 = -2\sqrt{2\varepsilon_S N_D(\psi_{bi} - kT/e)/e}$. Under the assumption $n_{in} \ll n_0$, ΔE_F can be expressed as

$$\begin{aligned} \Delta E_F(V) &= \frac{h}{4\sqrt{\pi}} v_F \frac{1}{\sqrt{n_0}} (n_g - n_0) \\ &= a \left(\sqrt{\left(\psi_{bi} - N - \frac{kT}{e}\right)} - \sqrt{\psi_{bi} - \frac{kT}{e}} \right) \end{aligned} \tag{3.6}$$

with $a \equiv \frac{h}{4\sqrt{\pi}} v_F \sqrt{\frac{\varepsilon_S N_D}{2en_0}}$.

The variation of the Fermi level corresponds to an opposite variation of the Schottky barrier $\Delta\Phi_B(V) = -\Delta E_F(V)$. If Φ_{B0} and $\Delta\Phi_B$ are the zero bias Schottky barrier and the correction of the zero bias Schottky barrier due to the applied voltage V, then the dependent Schottky barrier height can be written as:

$$\begin{aligned}\Phi_B(V) &= \Phi_{B0} + \Delta\Phi_B(V) = \Phi_{B0} - \Delta E_F(V) \\ &= \Phi_{B0} - a\left(\sqrt{\psi_{bi} - V - \frac{kT}{e}} - \sqrt{\psi_{bi} - \frac{kT}{e}}\right).\end{aligned} \tag{3.7}$$

In the Schottky model, the constant Φ_{B0} appears in the expression of the reverse current saturation current. By replacing Φ_{B0} with $\Phi_B(V)$, the Schottky barrier model equation, equation (1.61) and (1.60) can be rewritten as

$$\begin{aligned}I_0 &= AA^*T^2 \exp\left(\frac{\Phi_{B0} + \Delta\Phi_B(V)}{kT}\right) \\ &= AA^*T^2 \exp\left(\frac{1}{kT}\left[\Phi_{B0}\right.\right. \\ &\quad \left.\left. - a\left(\sqrt{\psi_{bi} - V - \frac{kT}{e}} - \sqrt{\psi_{bi} - \frac{kT}{e}}\right)\right]\right)\end{aligned} \tag{3.8}$$

and

$$\begin{aligned}I = I_0\left(\exp\left(\frac{e(V - IR_S)}{\eta kT}\right) - 1\right) \\ = AA^*T^2 \exp\left(\frac{1}{kT}\left[\Phi_{B0}\right.\right. \\ \left. - a\left(\sqrt{\psi_{bi} - V - \frac{kT}{e}}\right.\right. \\ \left.\left. \left. - \sqrt{\psi_{bi} - \frac{kT}{e}}\right)\right]\right)\left(\exp\left(\frac{e(V - IR_S)}{\eta kT}\right) - 1\right)\end{aligned} \tag{3.9}$$

From equation (3.8) Φ_{B0} can be still evaluated from the reverse saturation current I_0 at zero bias while $\Delta\Phi_B(V)$ can be evaluated from the variation of Φ_B at given V.

Equation (3.9) maintains the general form of the diode equation and includes the bias dependence of the reverse saturation current resulting from the Schottky barrier variation caused by the limited number of states of graphene around the Dirac point.

3.1.1 Graphene/Silicon Photodetector

Graphene/n-Silicon Schottky diode can be used as photodetector when operated under reverse bias. The optical absorption takes place mainly in the semiconductor while the graphene act as optically transparent and anti-reflecting carrier collector. The charges are photogenerated in the silicon depletion layer and in the graphene, but in the latter, they tend to recombine almost immediately and do not contribute to the photocurrent [16]. In dark and at low optical power, the Gr/Si junction shows the typical I-V of a photodiode, Fig. 21 (a), while at higher optical power the I-V shows an anomalous behaviour, Fig. 21 (b). The Gr/Si junction photocurrent gets smaller when the bias gets close or it is 0 V instead of following the typical diode behaviour, here plotted by the red dash line.

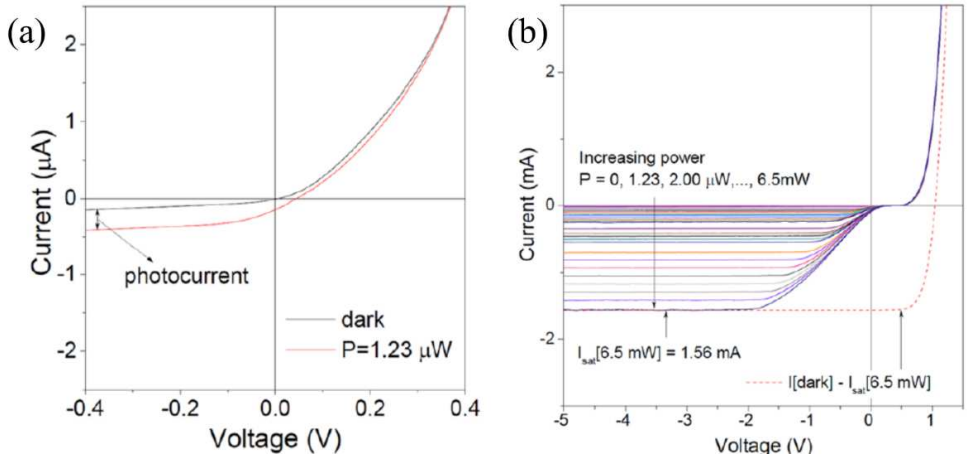


Fig. 21 (a) I-V characteristic of the diode reported in [35] measured in dark, low optical power and (b) high optical power.

This phenomenon was explained by considering the graphene band-gapless and conic band structure. At lower illumination power level, the graphene density states are enough to accept all the injected photocharges from the Silicon and the junction follows the classical photodiode behaviour along all the bias range. While at high illumination level and small $|V|$, the graphene density states are not enough to accept all the photogenerated charges limiting the photocurrent. By increasing the negative bias, the graphene Fermi level is shifted up and further density states are opened make the graphene able to accept all the photocharges.

Let's consider now what happens in a Gr/n-Si junction band structure at a fixed negative bias and illuminated with different photon energies [16,18,43]. If the photons energy is $h\nu > \Phi_B$ charges are photogenerated in the depletion layer and contribute to the photocurrent, while if the $h\nu < \Phi_B$ the charges are photogenerated in the graphene. The possibility to shift the E_F, and thus the Φ_B, allows the junction to detect different wavelength by simply tuning the bias.

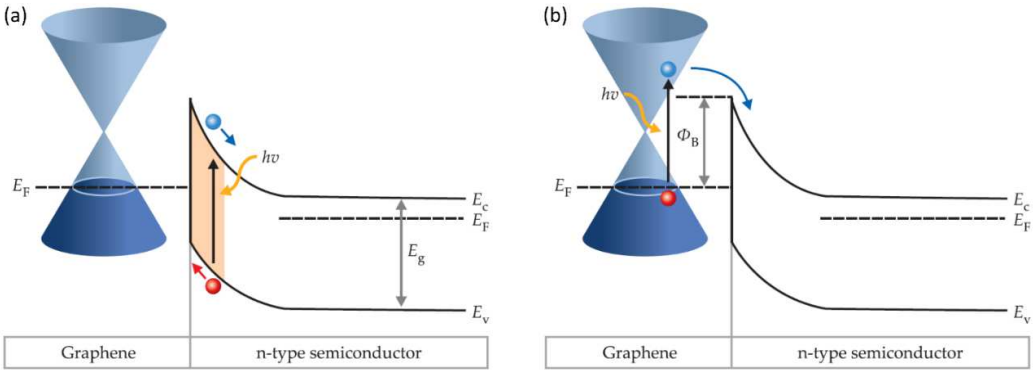


Fig. 22 Band structure of the Gr/Si junction when illuminated by a photon with (a) energy $h\nu > \Phi_B$ and (b) $h\nu < \Phi_B$.

3.2 Graphene/n-Silicon Planar Junction

3.2.1 Device fabrication

Graphene n-doped silicon planar junction (Gr/n-Si) was fabricated using a low n-doped silicon wafer ($\sim 4.5 \times 10^{14} cm^{-3}$) as substrate. The preparation starts with the formation of 15 nm-thick thermal SiO_2 layer which is followed by the CVD deposition 200 nm-thick SiO_2 layer. In the next step, a 10 μm-wide trench is patterned by lithography, dry SiO_2 etching is performed. The thermal SiO_2 is removed from the trench area with a hydrofluoridric acid dip before the graphene transfer to prevent the growth of native oxide. A CVD-graphene layer of $\sim 1 \times 0.4\, cm^2$ is transferred from a Cu foil on the substrate covering the Si trench and part of the oxide layer. After the etching treatment the oxide layer is 50 nm. Ohmic metal contact on graphene (Gr) is fabricated by evaporating of Ti/Au metal stack trough a shadow mask. Finally, a top-contact the Si-substrate is established depositing Ag paste on the exposed areas of the wafer, opportunely scratched to guarantee ohmic contact.

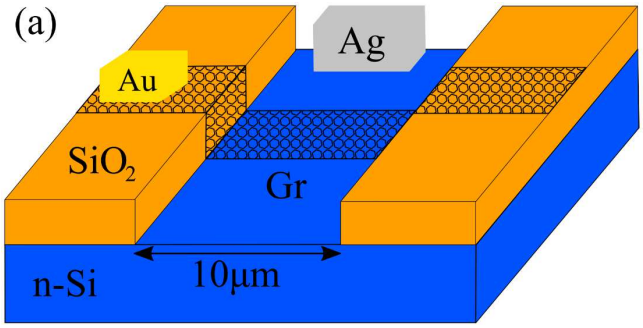


Fig. 23 (a) 3D schematic view of the Gr/n-Si diode.

Fig. 24 (a) shows a scanning electron microscopy (SEM) image of the trench edge after the graphene transfer. The characteristic graphene wrinkles extending across the edge of the trench from the isolated area as well as on the Gr/n-Si junction area are visible. Gr layer covers the edge of the trench keeping its structural integrity and ensuring electrical contact between the junction area and the contact area on top of the isolation layer. A darker region ($\sim 100 \div 200\, nm$ wide) extending along the trench wall indicates that graphene may be

freestanding in this region. As the latter area constitutes a negligible fraction of the Gr/n-Si junction area it is assumed for simplicity that the entire trench region is uniformly covered with Gr.

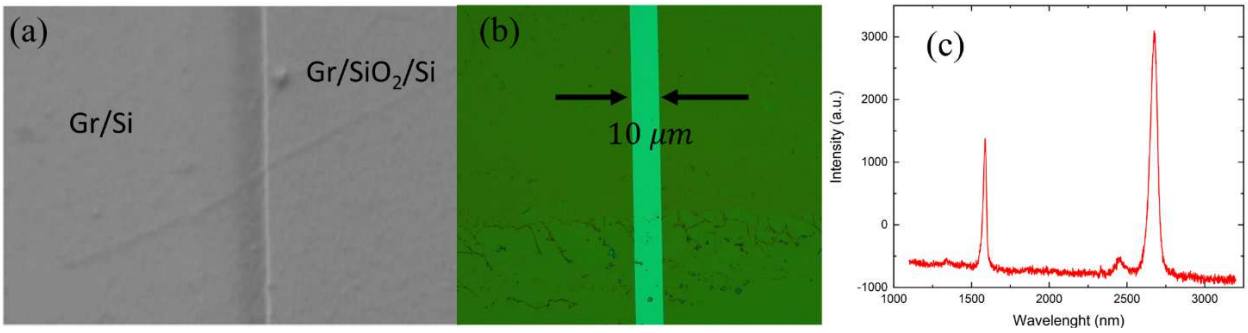


Fig. 24 (a) SEM image of the step between the trench and the insulator layer both covered with graphene. (b) Optical microscope image of the trench. (c) Raman spectra of the graphene on the SiO_2.

Fig. 24 (b) and (c) shows an optical microscope image of the trench covered with graphene and the Raman spectra performed on the $\mathrm{gr/SiO_2}$ close to the trench. The Raman spectra shows a very small D-peak ($\sim 1350\ cm^{-1}$ and two clears peak at $\sim 1568\ cm^{-1}$ and $\sim 2680\ cm^{-1}$ which indicates that the graphene layer is of good quality. Electrical and optical measurements were performed in a high-vacuum, cryogenic Janis probe station connected to a Keithley 4200 SCS parameter analyser. The forcing bias was applied to the Au/Ti contact on graphene, while the Ag pad on Si was grounded. To avoid moisture or particulate deposition on the surface, the sample was kept in vacuum ($< 10^{-3}\ mbar$) at room temperature for 2 days or more, and kept below $50\ mbar$ in rest gas atmosphere during the measurements.

3.2.2 Device electrical characterization

Fig. 25 (a) shows the semi-logarithmic plot of the I-V characteristic of the device, measured in dark after 2 days of vacuum annealing at $50\ mbar$ and at different temperature from 310 K to 402 K.

The device exhibits a clear rectifying behaviour, with rectification ratio up to 10^3, quasi-saturated reverse current and forward current exponentially growing till the reach of a downward bending region. As we explained in the previous chapter, the reverse saturation current I_0 and the ideality factor η can be determinated from the linear region of the forward current of the I-V. Assuming that A^* is the same of a metal/Si junction, $112\ A \cdot cm^{-2}K^{-2}$, we obtain a Schottky barrier value of $q\phi_B \sim 0.9\ eV$ and an ideality factor $\eta = 3.83$.

The red dash line in Fig. 25 (a) shows that equation (2.60) fails to reproduce the reverse saturation current which appears to be 2-3 order of magnitude lower than the one we measured. The same phenomenon has been observed by Di Bartolomeo et al. in [27] and was partially resolved by rewriting the ideal diode equation adding the lump resistance, which is the total resistance of the graphene layer, the silicon substrate and the Au and the Ag contact. Although the model they introduce failed to reproduce the I-V characteristic at room temperature, it was able to reproduce the I-V at lower temperature. These results suggest that the Gr/Si reverse saturation current possesses also a thermo-current component which, as we will see in the next chapter, affects the graphene Fermi level and thus the Schottky barrier.

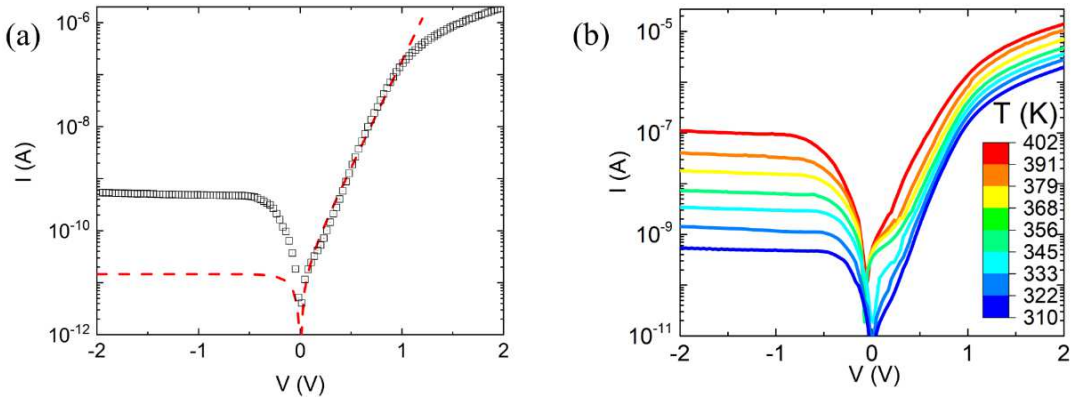


Fig. 25 (a) I-V characteristic of the Gr/n-Si diode and fitting equation (Thermionic) (red dash line) and (b) I-V characteristic of the Gr/n-Si for increasing temperature from 310 K to 400 K at pressure of ~ 50 mbar.

The Schottky barrier height $q\phi_B$ we obtained is higher than the one reported in literature for low n-doped silicon substrate [46,109–113]. This overestimation is probably due to the Richardson constant A^* value that we used. According to the experimental evidence, this value could be several order smaller raging from 10^{-1} to 10^{-3} [28,112,114]. Following what we said in the paragraph 2.6, it is possible to determinate both $q\phi_B$ and A^* from the Arrhenius plot, equation (2.63), of the $\ln(I_0/T^2)$ respect the T^{-1} (Fig. 26 (a)).

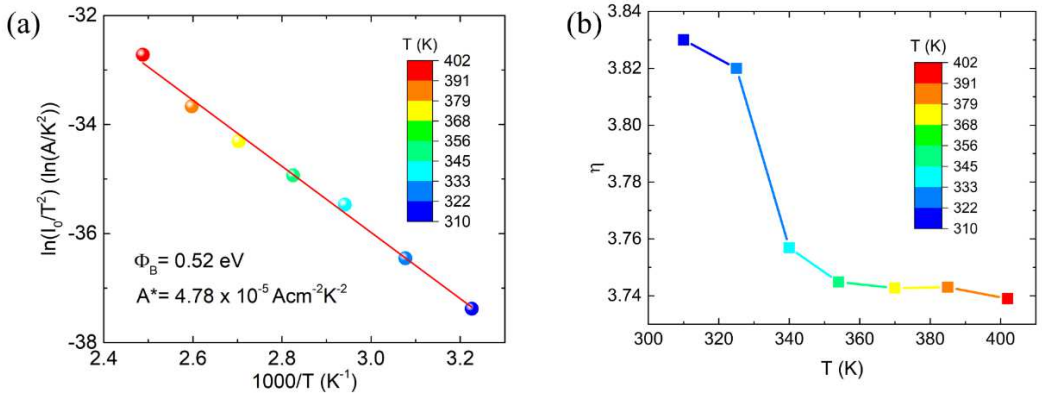


Fig. 26 (a) Richardson plot of $\ln(I_0/T^2)$ vs $10^3/T$ to extract the barrier height. (b) Ideality factor η measured from the forward current at each temperature.

We obtain a Schottky barrier of $q\phi_B = 0.52\ eV$ and a Richardson Plot of $A^* = 4.78 \cdot 10^{-5} A\ cm^{-2}K^{-}2$, which is 8 order of magnitude smaller than the one reported for this type of semiconductor. Although the origin of a lower $A^*$is still under debate, it has been observed that is usually accompanied by a high η, which indicates the presence of an oxide layer [27–32,102,115]. Since the graphene was transferred after the HF treatment, we can suppose the insulator layer is mainly formed by native SiO_2. From the equation (2.58), we can estimate the oxide layer thickness. By redefining the Richardson constant A^* as

$$A^{**} = A^* \exp\left(-\sqrt{\chi}\delta\right) \tag{3.10}$$

and $A^* = 112\ A \cdot cm^{-2}K^{-2}$ is the theoretical Richardson constant of metal/n-Si junction, $\chi \sim 3\ eV$ fro SiO_2. We estimated an oxide layer thickness of 8.5 Å. Indeed, X-ray photoelectron spectroscopy measurement (XPS) confirmed a SiO_x layer underneath graphene slightly differs from the native oxide on uncovered Si, with $x < 2$ and thickness

$\sim 1nm$. The presence of the interfacial layer reduces the majority-carrier thermionic emission current but does not affect the current due to the minority-carrier which diffuse.
Now that we have a reliable value for the Richard constant, we can determinate the series resistance R_S, $q\phi_B$ and η using the Cheung and Cheung method, described in paragraph 2.6.1.

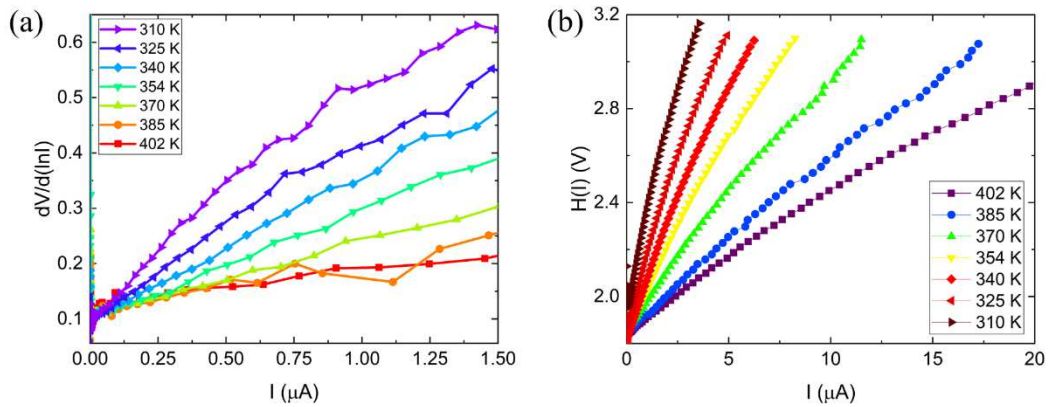


Fig. 27 Cheung plot of (a) $dV/d\ln(I)$ vs I and (b) $H(I)$ vs I at each temperature

Fig. 27 (a) and (b) display the $dV/d\ln(I)$ and $H(I)$ vs I plots from equation (2.65) and (2.67). We can observe that in both cases the slope gets smaller at higher temperature indicating a reduction of the R_S (Fig. 28(a)).

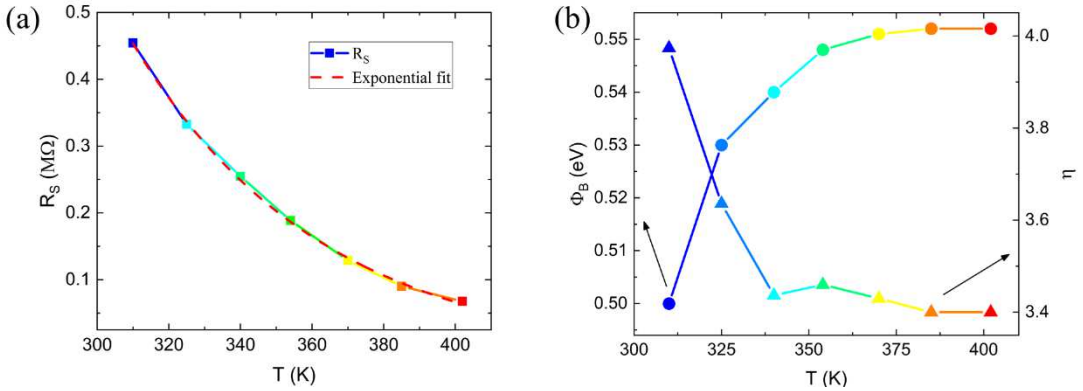


Fig. 28 (a)Gr/n-Si series resistance, (b) Schottky barrier and ideality factor extracted from the C. C. method.

The series resistance displays an exponential decrease with the T ($R_S \sim \exp(-\alpha T)$) typical of semiconductor with negative temperature coefficient of resistance (Fig. 28 (a)). This behavior cannot be attributed to the silicon substrate [116,117] nor the metal or the ohmic contact [118] so it can only be due to the graphene [119]. Similar behavior have been observed for CVD graphene both suspended [56] or deposited on substrate [120–122]. The negative temperature coefficient in graphene is the result of competing mechanisms, with the thermally activated transport through inhomogeneous electron-hole puddles as the main recognized cause [122]. From the C. C. model, we obtain a $q\phi_B \sim 0.5$ and $\eta \sim 4$ which is in agreement with the values we observed before.
The increase of the Schottky barrier and the decrease of the ideality factor respect the temperature confirm the thermionic emission is the dominant carrier conduction process at high temperature, while at lower temperature, the increase of η indicates the presence of other transport phenomena, such as the generation-recombination of charges in the depletion layer and tunneling through the barrier [27–29,102].

3.2.3 Optical characterization

To further investigate the underlying physical mechanisms of carrier transport, we tested the optical response of the device. Fig. 29 shows the I-V characteristics measured at room temperature, under exposure to the light from a white LED system with controllable intensity. The optical power was measured using a photometer placed at the same distance of the sample.

The Gr/n-Si diode shows a photocurrent, I_{ph}, higher than the forward one at higher illumination level. This feature is quite unusual in Gr/n-Si photodetectors and has been reported on few articles [27,29,33,34]. Also, a photovoltaic effect with $V_{oc} \approx 0.2\ eV$ at room temperature is observed. The photocurrent at given illumination reaches a plateau at high reverse bias, which is the indication of limited photo-carrier generation rate.

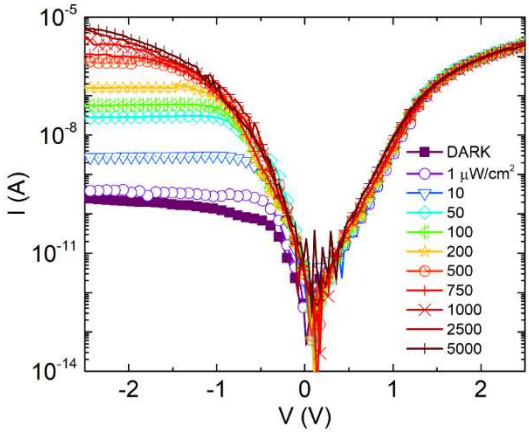


Fig. 29 (a) I-V characteristic measured at different illumination level

The plateau current exhibits a linear behavior with the optical power incident on the Gr/n-Si junction area, P_{opt}, as shown in Fig. 30 (a). Fig. 30 (b) displays the responsivity, defined as the ratio of the photocurrent to the incident power on the junction area, $\mathcal{R} = I_{ph}/P_{opt}$, as a function of P_{opt} and shows that a peak of 5 AW^{-1} is achieved.

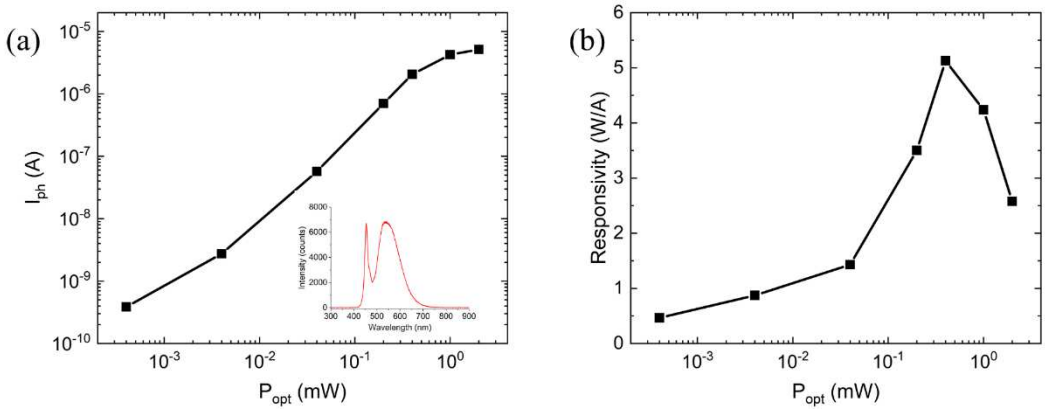


Fig. 30 (a) Photocurrent and (b) Responsivity as a function of the optical power incident on the junction area.

The spectrum of the LED light extends over the range $420 - 720\ nm$ (inset Fig. 30(a)). Considering the average wavelength $\bar{\lambda} = 545\ nm$, and assuming a constant responsivity $\mathcal{R}$ on such range, from

$$\mathcal{R} = \frac{I_{ph}}{P_{opt}} = \beta \frac{\lambda(\mu m)}{1.24} \qquad [A \cdot W^{-1}] \tag{3.11}$$

we estimate an external quantum efficiency, which is the number of carriers produced per incident photon, $\beta > 230\%$. Such high value is in agreement with other reports on similar devices [27,29,31,33,34].

3.2.4 Parasitic MOS Capacitor

The high photocurrent has been explained by considering the graphene/SiO_2/silicon MOS capacitor connected in parallel with the Gr/Si Schottky diode [27,29,31,33,34], Fig. 31.

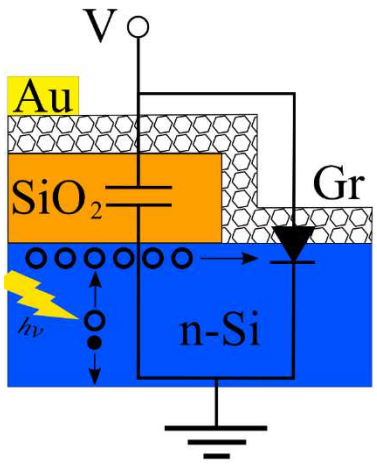


Fig. 31 Schematic view of the graphene/SiO_2/Si MOS capacitor connected in parallel with the graphene/Si junction when it is illuminated.

In forward bias the positive voltage on graphene causes accumulations of electrons at the SiO_2/Si interface of the MOS capacitor. These electrons do not affect the forward current since it is limited by the injection rate of electrons over the barrier. In reverse bias the electrons cannot overcome the barrier, and the saturation current is mainly due to minority carriers (holes). When the junction is illuminated e-h couples are photogenerated in the depletion layer and separated by the electric field. Under negative bias the MOS capacitor attracts the holes forming a reservoir at SiO_2/Si interface, and then they diffuse in the Schottky diode originating the photocurrent we observed. The holes motion is favoured by the band bending from the Gr/SiO_2/Si to the Gr/Si region as shown in Fig. 32.

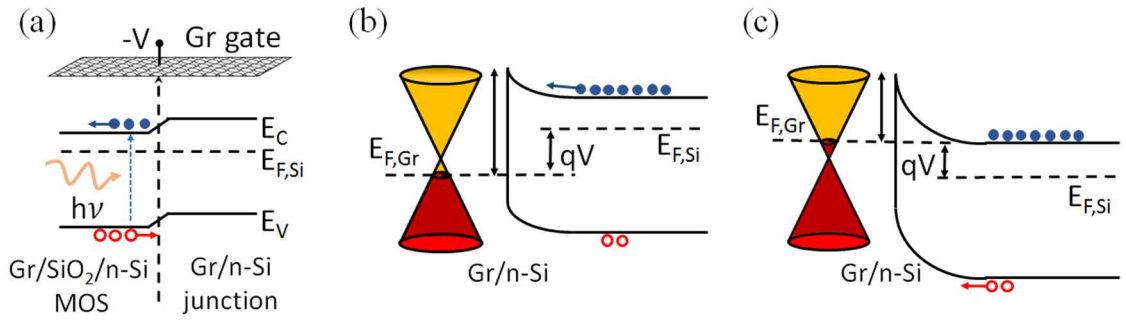


Fig. 32 (a) Band diagram of the n-type Si substrate along the surface below the Gr/SiO_2/Si MOS capacity and the Gr/Si diode, showing that diffusion of photogenerated holes towards the diode area is energetically favoured. Band diagram of the Gr/Si junction in (b) forward and (c) reverse bias.

It has been shown that the same mechanism, when applied to thermally generated minority carriers contributes to the high leakage of the Gr/Si junction [27]. To further investigate the carrier distribution in the Gr/n-Si diode we measured the Capacitance-Voltage (C-V) characteristic in dark and at the same illumination level we measured the I-V. The C-V were performed in the $-3\ V$ to $1\ V$ range DC bias range and with AC small signal of $100\ mV$ and $10\ kHz$ frequency.

Focusing on the dark curve (black solid line) in Fig. 33 (a), it can be noticed that the measured capacitance is dominated by the MOS capacitor, which is in accumulation, at positive bias. As the voltage is lowered below zero, the MOS enters the weak depletion region, which corresponds to a decreasing capacitance. However, a change in the capacitance behaviour occurs at $V \approx -0.25\ \mathrm{V}$, as highlighted in the inset of the Fig. 33 (a). The decreasing capacitance in the range $-2\ \mathrm{V} < V < -0.25\ \mathrm{V}$ is likely dominated by the depletion capacitance of the reverse biased Schottky diode. For $V < -2\ \mathrm{V}$, the quasi bias-independent capacitance indicates that the MOS, which is now in deep inversion, dominates again over the Schottky diode. Below $-2\ \mathrm{V}$, the minority carriers are not able to follow the 10 kHz oscillations, and the MOS is in deep depletion, with the capacitance at its lowest plateau value (the reverse-bias decreasing capacitance of the Schottky diode is negligible in this region). Under high illumination, electron-hole pairs are photogenerated in the depletion region and holes accumulate at the Si/SiO_2 interface forming an inversion channel, which raises the MOS capacitance to a value comparable to the one in accumulation at positive voltage. Otherwise stated, at the lowest biases and under high illumination, the device shows the typical C-V plots of a MOS on p-type semiconductor. This indicates that the photogeneration rate is able to provide enough positive charge to invert the n-Si and that the channel can follow the oscillation of the small ac signal.

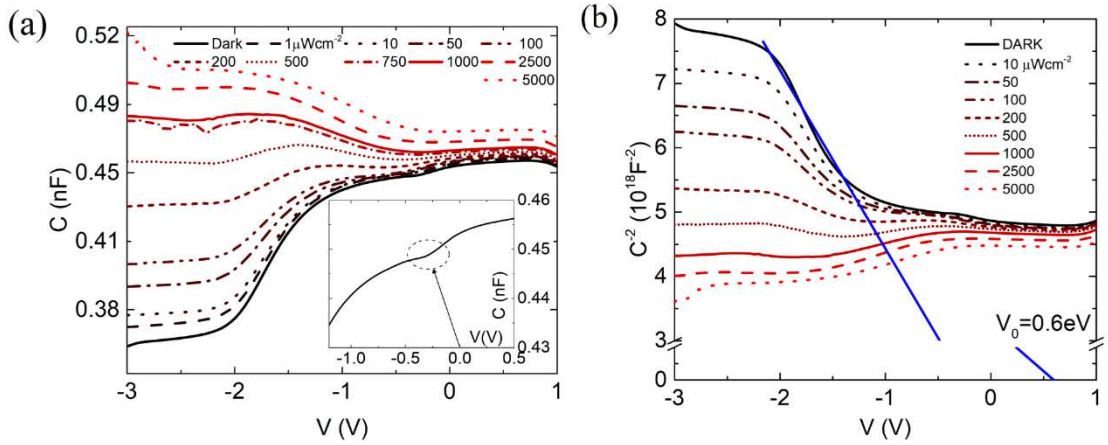


Fig. 33 (a) Small-signal (100 mV and 10 kHz) C-V measurements in dark and under different illumination levels. The inset highlights a crossover point between two regions where the capacitance of the device is dominated by the Schottky diode ($V < -0.25\,V$) and the MOS capacitor ($V > -0.25\,V$), respectively. (b) $1/C^2$ $-V$ plot of the device under study.

The holes of the inversion channel of the MOS capacitor, injected in the Gr/Si region, cause the high photocurrent of the device, as previously stated. The interpretation of the Gr/Si dominating capacitance in the range $-2\,V < V < -0.25\,V$ is confirmed by the linear behaviour of the $1/C^2$ vs. V plot, shown in Fig. 33 (b). For a Schottky non-ideal diode the inverse square of reverse-bias capacitance is a linear function of the bias [16,102]:

$$\frac{1}{C^2} = \frac{2n[n(q\phi_B - q\phi_n - \mathrm{k}T) - qV]}{A^2 q^2 \varepsilon_S N_\mathrm{d}}, \tag{3.12}$$

where N_d is the doping density, $\varepsilon_S = 11.7\varepsilon_0$ is the silicon permittivity, and $q\phi_n = kT \ln\left(\frac{N_c}{N_d}\right)$ with $N_\mathrm{c} = 12(2\pi m^* \mathrm{k}Th^{-2})^{3/2}$, the effective density of states in the conduction band. According to Equation (3.12), the barrier height $q\phi_B$ can be evaluated from the x-intercept, V_0, of the straight line fitting the $1/C^2$ pòvs. V plot and results

$$q\phi_B = \frac{V_0}{\eta} + \mathrm{k}T \ln\left(\frac{N_\mathrm{c}}{N_\mathrm{d}}\right) + \mathrm{k}T \approx 0.47\mathrm{eV}, \tag{3.13}$$

($N_\mathrm{d} = 4.5 \times 10^{14}\mathrm{cm}^{-3}$ is the substrate doping and $\eta = 3.8$ is the measured room-temperature ideality factor). The obtained value of $q\phi_B$ is close to the barrier height extracted from the Richardson's plot and from the Cheung's method.

3.3 Gr/p-Silicon planar junction

3.3.1 Device fabrication

The Gr/p-Si Schottky diode was fabricated following the same method used for the Gr/n-Si Schottky diode described in the paragraph 3.2.1, but in this case, a p-doped silicon wafer with a boron concentration of $\sim 4.5 \times 10^{14} cm^{-3}$ was used as substrate. And the insulator layer is a $\sim 50\,nm$-thick SiO_2 layer CVD growth. A schematic view of the device is shown in Fig. 34 (a). The device I-V characteristic was measured with the two-probe method using

a Keithley 4200 SCS and a cryogenic Janis Probe station at the controlled pressure of 5 $mbar$.

3.3.2 Electrical characterization

Fig. 34 (b) displays the I-V characteristics measured in the temperature range from 400 K to 180 K. In order to stabilize the thermal conditions, the electrical measurements were delayed by 20 min at each temperature step. The voltage was applied to the Gr (anode) while the Si substrate (cathode) was grounded (we have reversed the voltage in Fig. 34 (b) for convenience in the data analysis). Below 1 V, the forward as well as reverse currents increase exponentially with the applied voltage, although the reverse currents increase with about a half the rate. The device demonstrates rectification behaviour, with a modest rectification factor of few tens at $\mp 0.5\ V$, which increases to $\sim 10^2$ at lower temperatures ($\sim 200\ K$). The device reverse current shows a plateau at low temperature (Fig. 34(b)), which extends at higher reverse biases while reducing the temperature.

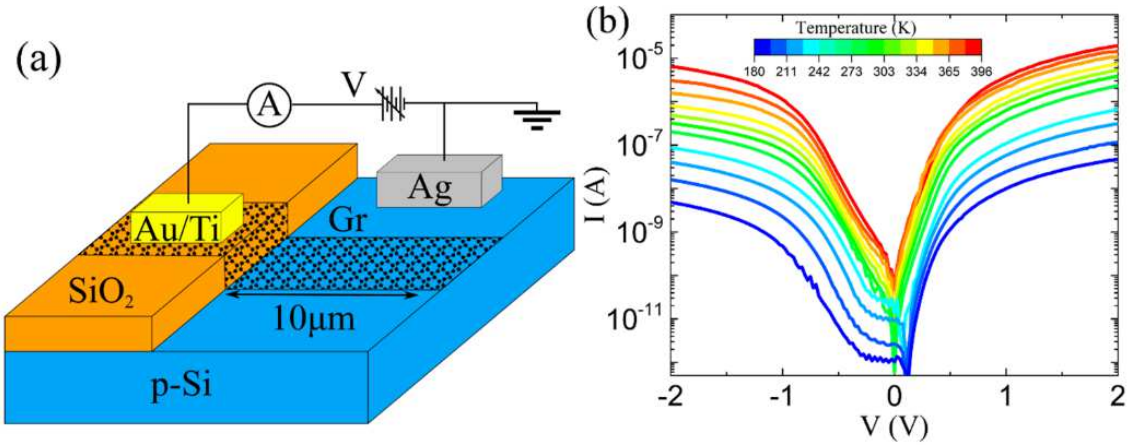


Fig. 34 (a) 3D schematic view of the Gr/p-Si device. (b) I-V characteristics of the Gr/p-Si junction measured from 400 K to 180 K at 5 mbar. The voltage was applied to graphene (anode), while the Si substrate (cathode) was grounded; we have reversed the voltage in the figure for the convenience of the analysis.

Following the same method, we described in paragraph 2.6 and applied before for the Gr/n-Si junction, we determinate the η at different temperature, Fig. 35 (a). Also, in this case, we can observe a higher η for lower temperature which it gets smaller by increasing the temperature. At lower temperature the current is mainly due to tunneling and diffusive mechanism (higher η), while at higher temperature the T.E. (lower η) is stronger. From the Richardson Plot of the saturation current I_0 measured at each temperature vs $1/T$, we obtained $q\phi_B = 0.18\ eV$ and $A^* = 9.08 \cdot 10^{-10}\ Acm^{-2}K^{-2}$. The points at lower temperatures are excluded from the fitting, since significant deviation from thermionic regime occurs at low temperatures. Also, in this case, we obtained a lower Richardson constant (which is $\approx 32\ A \cdot Acm^{-2}K^{-2}$ for p-Si substrate) which indicates the presence of an insulator layer.

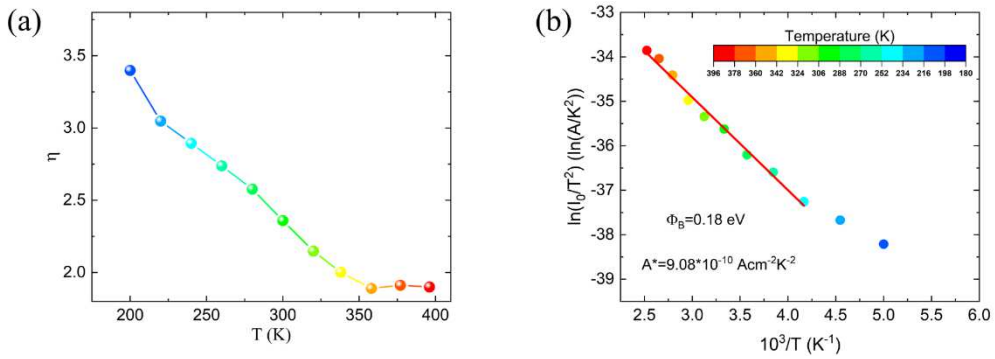


Fig. 35 (a) Ideality factor versus temperature and (b) Richardson plot of $\ln(I_0/T^2)$ versus $10^3/T$. Some points have been excluded from the fit since significant deviation from thermionic behaviour usually occurs at low temperatures.

Since the fabrication process is the same for Gr/n-Si and Gr/p-Si, the insulator layer is made mainly of SiO_2. From equation (3.10) we estimated a 16 Å SiO_2 layer thick. The presence of an oxide layer of the estimated thickness at the Gr/Si interface is confirmed by the x-ray photoemission spectra, shown in Fig. 36, which compares Si trench regions covered and uncovered by graphene.

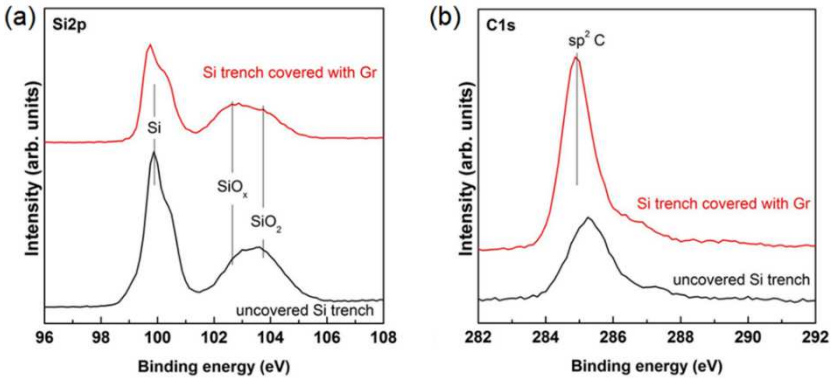


Fig. 36 Si 2p (a) and C 1s (b) x-ray photoelectron spectra acquired on graphene-covered Si trench and on uncovered Si trench. Exposure to ambient conditions causes oxidation of the Si junction areas underneath Gr where mostly Si sub-oxides are formed (SiO_x, $x<2$). On the uncovered areas Si oxidizes mostly to SiO_2.

At high forward bias or reverse bias $|V| > \sim 1V$, the I-V characteristic shows a bend which is due to the series resistance, R_S. Using the C. C. method [106], we plotted the $dV/d(\ln I)$ vs I and $H(I)$ vs I at each temperature (Fig. 37 (a) and (b)) and extrapolated the $q\phi_B$, η and R_S. We obtain $q\phi_B = 0.17\ eV$ and a series resistance ~ 500 kΩ at room temperature.

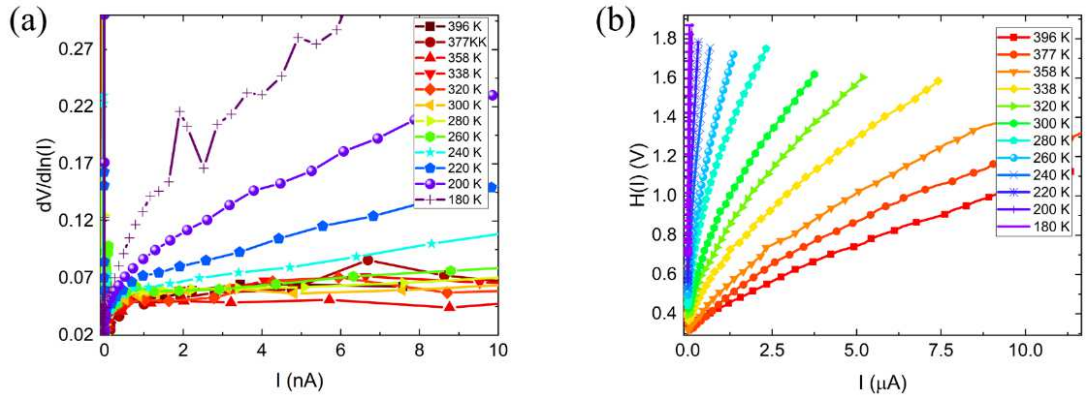


Fig. 37 Cheung's plot of (a) dV/dln(I) vs I and (b) H(I) vs I obtained at each temperature.

The Schottky barrier height increases with temperature and reaches a maximum value around 270 K, after which it becomes temperature insensitive (Fig. 38 (a)). The decrease of the $q\phi_B$ with decreasing temperature is an indication of spatial inhomogeneity of the graphene/Si junction, the $q\phi_B$ presenting peaks and valleys [28,31,123]. At higher temperature, the carriers possess enough energy to overcome the $q\phi_B$ peaks, while at lower temperature they are forced to pass through the valleys and a lower $q\phi_B$ is measured.

Fig. 38 (b) displays the Gr/p-Si series resistance exponential decrease respect the temperature, which is quite similar to the one we observed before for the Gr/n-Si and we attribute to the graphene [117,119,120]. In this case the variation (from 10^7 to 10^5 $M\Omega$)is much more visible since the temperature range is larger.

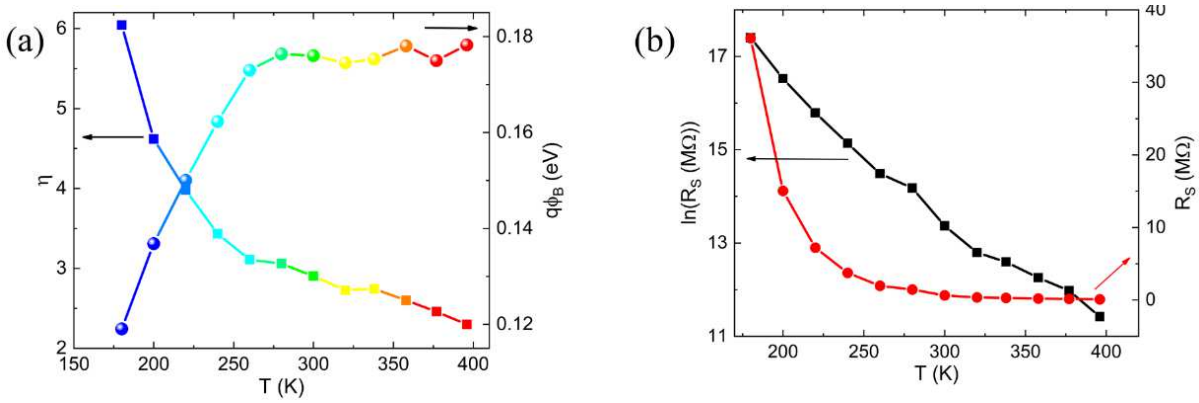


Fig. 38 (a) Ideality factor and Schottky barrier height and (b) device series resistance and $ln(R_S)$ vs temperature extracted from Cheung's method for $|V| > 1V$.

We conclude the electrical characterization by checking the value obtained using the modified Norde's method [107,108], equation (2.68), (2.69) and (2.70). $F(V_{min})$ and V_{min} were extrapolated from the plot $F(V)$ vs V displayed in Fig. 39 (a) for different γ values, I_{min} is the current value at the voltage V_{min}.

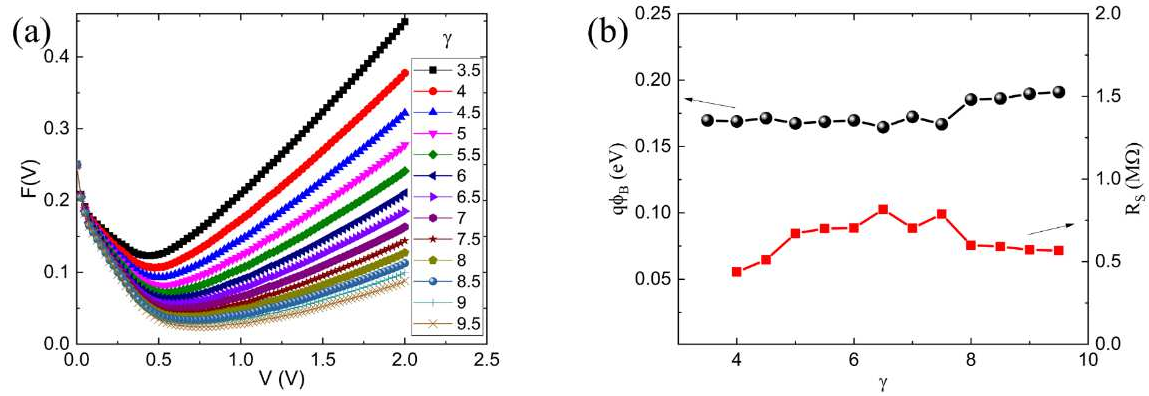


Fig. 39 Modified Norde's method (a) F(V) vs V plot for different values of γ, (b) The $q\phi_B$ (black circle) and the series resistance R_S (red square) computed from the Norde's method.

Fig. 39 (b) displays the $q\phi_B$ and the series resistance, obtained from equation (2.70) with the η used from the Thermionic emission model and shows that the extracted value is independent of γ. Norde's method provides a $q\phi_B = 0.17$ eV and a series resistance $R_S \sim 600\ k\Omega$ at room temperature, consistent with the ones extracted using the other two methods.

The low $q\phi_B$ is due to the well-known p-type doping of graphene. Many causes have been reported to contribute to the p-doping of graphene (see paragraph 1.4). One of these is the PMMA which can leave residues on the graphene sheet and induce a p-type doping [74]. Air exposure is a well-known cause of graphene p-doping. An additional source can be the boron diffusion from the substrate into the graphene layer during the temperature ramp up, as we will discuss in the following.

To explain the observed I-V-T behaviour we propose the band model shown in Fig. 40 [30]. The band alignment in unbiased condition is pictured in Fig. 40 (a), showing graphene and Si lightly p-doped. In forward bias, i.e. for a negative voltage applied to the graphene contact with respect to Si, the Fermi level of graphene (E_{gr}) is raised with respect to the Si Fermi energy (E_{FS}), causing the barrier height ($q\phi_i$) for holes moving from Si to graphene to be reduced by the amount qV/η (where V is the applied voltage and n the ideality factor), as shown in Fig. 40(b). Furthermore, due to the low density of states of graphene, the Fermi level of graphene is up-shifted with respect to the double cone, that is graphene becomes less p-doped, since there is reduced negative space-charge at the Si interface to mirror in graphene. This condition results in increased $q\phi_B$, as shown in Fig. 40 (b). In reverse bias, which is for positive voltage on graphene, the Fermi level of graphene is lowered with respect to that of Si. The graphene Fermi level is down-shifted along the double cone, because the p-doping of graphene increases to counterbalance the augmented negative space-charge in Si. This situation corresponds to a decreasing $q\phi_B$, as shown in Fig. 40 (c) and (d) for raising reverse bias at low and high voltages, respectively. The decreasing $q\phi_B$ due to bias (likely contributed also by image force barrier lowering [28], here not explicitly pictured) is the cause of the exponentially increasing reverse current, as reported also elsewhere [16,27–29,31,124]. The Si bandgap suppresses the injection of holes from graphene until the reverse bias aligns E_{gr} with the upper level of the Si valence band (E_V), as shown in Fig. 40 (c). However, the suppression of current, which manifests itself as a plateau in the reverse I-V characteristics, becomes evident only at lower temperatures, when the Fermi distribution function becomes more step-like and the Fermi window for conduction is reduced.

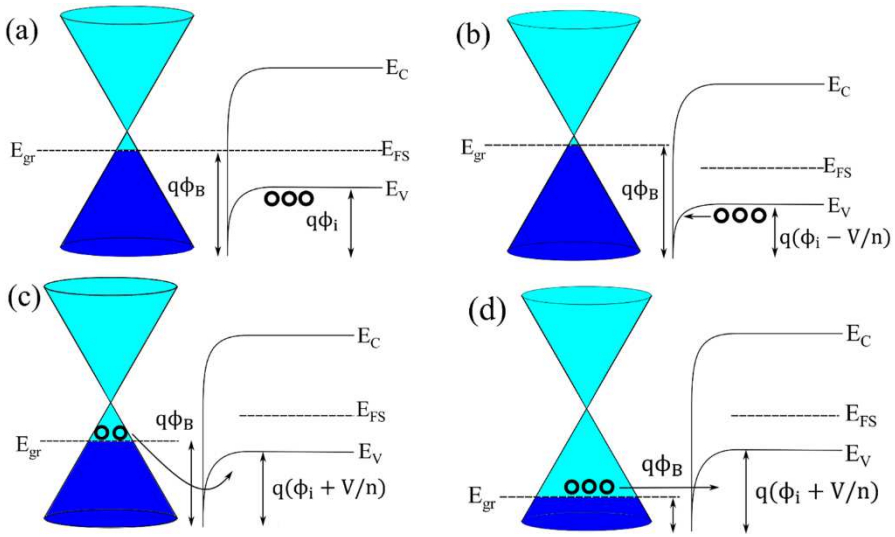


Fig. 40 Band diagram of the Gr/p-Si heterojunction, with symbols having the usual meaning, in (a) unbiased condition, (b) forward bias and reverse bias with (c) lower and (d) higher applied voltage. Charge carriers (holes) are shown as open circles. The interfacial tunnelling oxide layer is not shown for simplicity.

Otherwise stated, at lower temperatures, the current due to hot holes (with energy below E_{gr}) is negligible and very low current is detected until the reach of the E_{gr}-E_V alignment condition. After that, energy states become available in Si, and injection of holes from graphene can take place, thus originating the observed high reverse current.

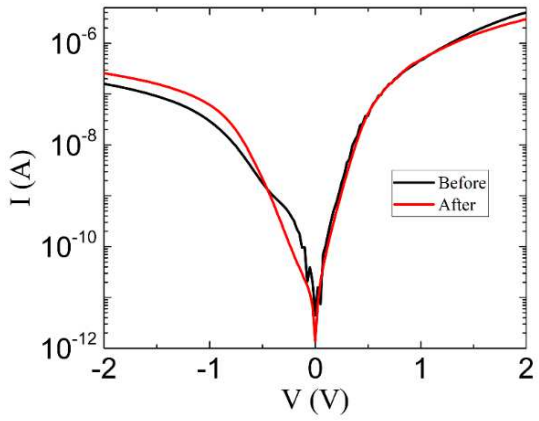


Fig. 41 Room-temperature I-V characteristics of the device measured before and after the temperature ramp up.

Fig. 41 shows a comparison of the I-V characteristics measured at room temperature before and after the high temperature ramp up to 400 K. The I-V characteristic of the as-produced device presents at room temperature a small knee in reverse bias down to $\sim -0.4\,V$ (black line in Fig. 41), which disappears after the device is subjected to the high temperature measurement cycle. This feature is more evident as plateau at low temperature, as previously shown in Fig. 34 (a). Referring to the band model of Fig. 40, the disappearance of the plateau suggests that the p-doping of graphene has increased after the high temperature annealing (made before the temperature ramp down) favouring the E_{gr} to Si E_V upper-level alignment condition (Fig. 40 (d)). Since the device was kept in the probe-station chamber at constant pressure during the I-V-T measurements, the temperature annealing treatment is likely the main cause of this extra doping. Indeed, a recent study has demonstrated that p-doping of graphene on boron-doped Si substrates occurs after a 3 h annealing at the temperature of 400

K, by incorporation of B or Si atoms in graphene vacancy sites [47]. This process likely took place in our device, which was subjected to similar annealing conditions. This extra doping can explain the slightly lower Gr/p-Si $q\phi_B$ measured in the present work compared to other studies and why the reverse curve of the device shows a clear plateau only at the lowest temperatures.

3.3.3 Optical Characterization

Finally, Fig. 42 shows the current voltage characteristics of the device under different illumination levels by a white LED system, measured at room temperature and 5 mbar. A photocurrent appears only in reverse bias, thus confirming the Schottky behaviour of the junction. At the reverse bias of $0.5\,V$ and with the incident optical power $P_{opt} = 5\,mW/cm^2$, the device exhibits a responsivity $R \approx 0.05$ A/W. At higher voltages the responsivity increases until reaching the value of 2 A/W at -2V. Despite the good responsivity the use of the device as photodetector is hindered by the high dark current which results in high power consumption and reduced sensitivity to low intensity radiation.

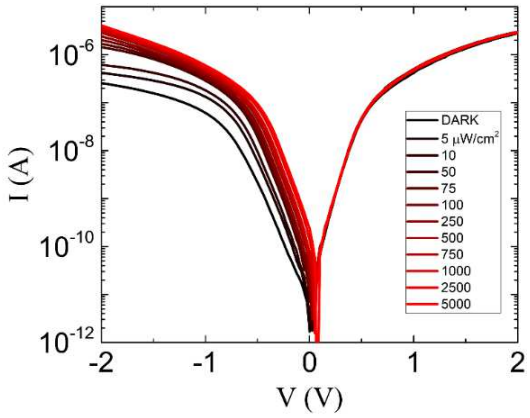


Fig. 42) I-V characteristics of the Gr/p-Si junction under different illumination levels from a white LED array.

We remark that the reverse current of the device increases with increasing light intensity up to almost exceeding the forward current. We observed the same behaviour in the Gr/n-Si planar junction and we attributed this phenomenon to the parasitic Gr/SiO_2/Si MOS, which is in parallel with the gr/Si Schottky diode, acts as a reservoir of photogenerated minority carriers which accumulate at the Si/SiO_2 interface under reverse bias [27,29,31,33,34].

3.3.4 Conclusion

In conclusion, we fabricated and characterized two Gr/Si Schottky diode which differ only for the substrate type doping. We observed that the Gr/n-Si displays a rectification factor of three order of magnitude along all the measurement range, $\pm 2\,V$ at room temperature, while the Gr/p-Si shows a rectification of on order of magnitude only in a small part of the range, $\pm 0.5\,V$ out of $\pm 1.5\,V$ which increase of one order at low temperature. We explained this result by taking in account the graphene doping and thus the position of its Fermi level. When exposed to the atmosphere graphene tend to p-doped, because of that its Fermi level is below the Dirac point, so when it is joint with a n-doped silicon substrate, the difference between the graphene Fermi level and the silicon electron affinity is big enough to assure a good Schottky barrier. In the case the graphene is joint with a p-doped silicon substrate, the

graphene Fermi level is too close to the silicon valence band forming a small Schottky barrier. We also observed that p-doped silicon substrate tends to p-doped the graphene when the junction is exposed at high temperature for long time. The boron atoms in the p-silicon crystal are weakly bonded to the silicon atoms, because of that, the rise of the temperature gives enough energy to the boron atoms to break free and move in a free spot in the graphene layer. The presence of boron atoms in the graphene lattice induce a p-doping which lowers the graphene Fermi level further making it even closer to the silicon valence band. This result suggest that a Gr/n-Si junction is more rectifying and durable than a Gr/p-Si junction. We conclude this chapter by considering the high responsivity both devices show when they are exposed to the white LED light. We attributed this behaviour to the graphene/SiO_2/Si MOS capacitor which forms a reservoir of charges when a reverse bias is applied. This result is very important, since it suggests that is possible increase the junction responsivity by connecting a MOS capacitor in parallel.

4 Graphene/Patterned Silicon Substrate Schottky Diode

A planar junction geometry with a low n-doped Silicon substrate and a parallel MOS capacitor have proven to be the best choice to realize a stable over time high sensible photodetector. It looks like the device structure can affect, even if not directly, the Gr/Si junction. In this chapter we are going to study what happen if the substrate is not planar.

4.1 Graphene/pillar Silicon Junction

4.1.1 Device fabrication

Fig. 43 (a) shows the schematic view of the Gr/Si-pillar junction. Three silicon square pillar with different surface were patterned from a highly doped n-doped Si ($\sim 10^{18} cm^{-3}$) substrate by photolithography. The pillars are $\sim 500\ nm$ height and the edges are $30\ nm$, $50\ nm$ and $100\ nm$ long. Although the pillars present different surface, their perimeter/area ratio ($\sim 10\%$) is similar for all of them. We can aspect them to behave similar. A SiO_2 layer was CVD-deposited until it covered the silicon pillar. CMP was then used to remove the oxide layer on the pillars top. A commercial graphene layer was transferred from Cu foil on the pillar with wet transfer process. The ohmic contact on graphene (anode) was realized by evaporating Au on it, while the other contact (cathode) was formed by coating silver paste on the scratched back-side of the Si substrate. Fig. 43 (b) shows a microscope image of the graphene/pillars top, we can observe the typical graphene wrinkles spreading on the pillar surfaces and oxide layer.

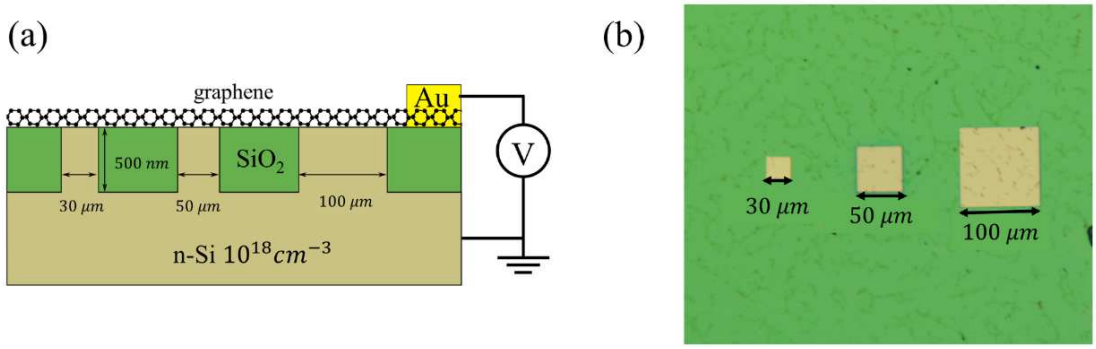


Fig. 43 a) 2D Schematic view of the gr/Si-pillar device. b) Optical microscope image of the pillars.

The Raman spectrum of the graphene transferred on the substrate was measured on the SiO_2 and Si pillars and it shows a clear peak at $\sim 1568\ cm^{-1}$ and $\sim 2680\ cm^{-1}$ which indicates that graphene is a good quality monolayer.

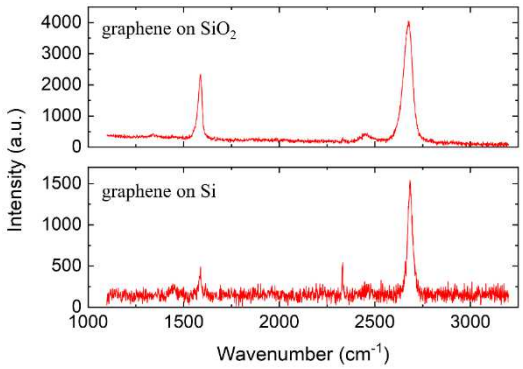


Fig. 44 Raman spectroscopy of the graphene on SiO_2 and Si. The big difference between the two spectra is due to Si high absorption respect the SiO_2.

4.1.2 Electrical characterisation

Fig. 43 (d) shows the I-V characteristics measured for the Gr/Si-pillar junction at different temperatures in the range $200 - 400\,K$ at $1\,mbar$ and in dark. From low to room temperature the Gr/Si-pillar junction shows an exponential reverse current which is typical of Gr/Si junctions [16,27,30,45,49]. At higher temperatures, after the initial fast growth of the ohmic regime at low bias, the reverse current exhibits a gradual weaker dependence on the bias until it becomes quasi-saturated. The I-V characteristic at room temperature shows a rectification factor of two order of magnitude at ± 1.5. The reverse current at lower temperature shows an exponential growth, which could be an effect of the graphene Fermi level shift due to its low-density state [28,35,46].

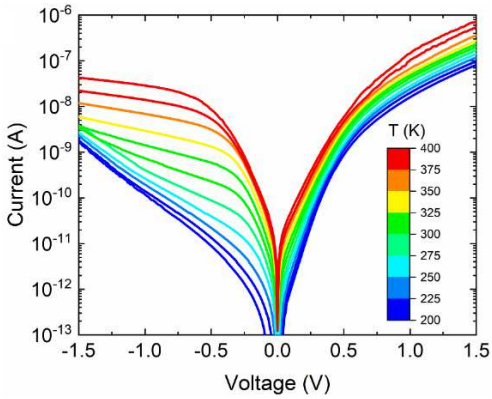


Fig. 45 d) I-V characteristic of the device measured from $200K$ to $400K$.

From the I-V characteristic we determinated the Schottky diode parameters using the T.E. theory and C.C. method (paragraph 2.6). In Fig. 46 (a) and (b) are shown the ideality factor η extracted at each temperature and the Richardson plot of the $\ln(I_0/T^2)$ vs $10^3 1/T$.

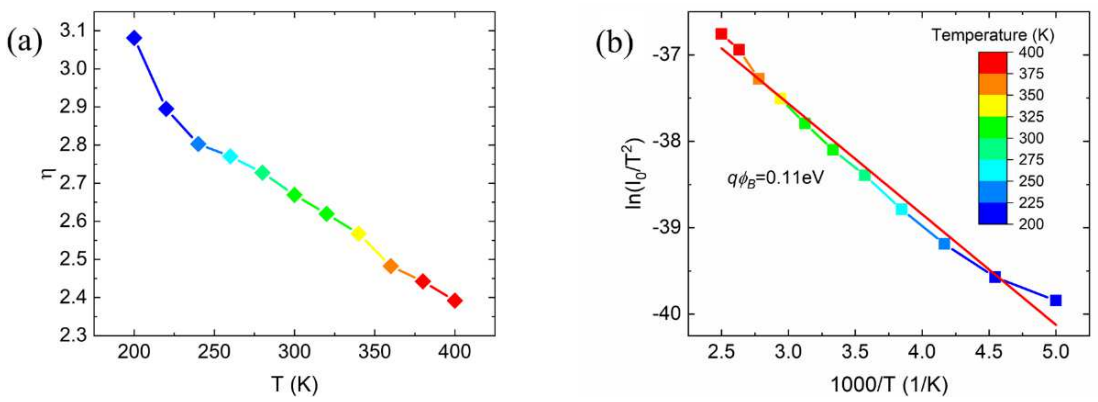


Fig. 46 a) Ideality factor vs the temperature extracted from the T.E. model b) Richardson plot of the $ln(I_0/T^2)$ *versus* $10^3/T$.

The ideality factor η decrease respect temperature increasing indicates that the current transport is mainly thermionic. The η values are in agreement with the ones we obtained for the other device, which suggest the presence of an oxide layer between the graphene and the pillars. From the linear fit of the Richardson plot, Fig. 46 (b), we obtained a $q\phi_B = 0.11\ eV$ and, a $A^* = 1.68 \cdot 10^{-9} A \cdot cm^{-2} K^{-2}$ which is also in agreement with the ones we obtained from the other devices, and it confirms the presence of the oxide layer. The oxide layer could be the native oxide which formed when the substrate was exposed to the atmosphere between the CMP process and the graphene layer deposition. From equation (2.58), we estimate an oxide layer of ~ 15 Å, which is thin enough to allow tunneling current, but can sustain a voltage drop and affect the I-V characteristic of the junction.

At higher voltage ($V \geq 0.8\ V$), the thermionic emission current is limited by the series resistance R_S. In order to determinate it, we used the C.C. method and extrapolated the $dV/d\ln(I)$ vs I and $H(I)$ vs I, Fig. 47 (a) and (b). And lastly from them we determinated the R_S, η and the $q\phi_B$ values at each temperature.

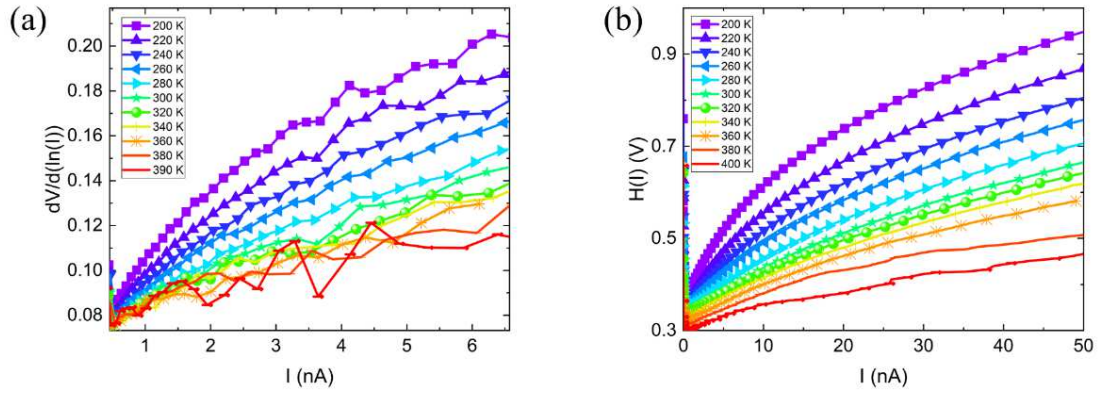


Fig. 47 Cheung's plot of a) $dV/d\ln(I)$ *vs I and b)* $H(I)$ *vs I at* 300K.

We estimated a $R_S \sim 10M\Omega$, a $\eta \sim 3$ and a $q\phi_B \approx 0.11\ eV$ at room temperature, which are in agreement with the previous evaluation. Also in this case, the series resistance shows an exponential decreasing respect the temperature, Fig. 48 (a), which can be attributed to the graphene [120–122]. The temperature growing $q\phi_B$ is an indication of possible spatial inhomogeneities which we will discuss later.

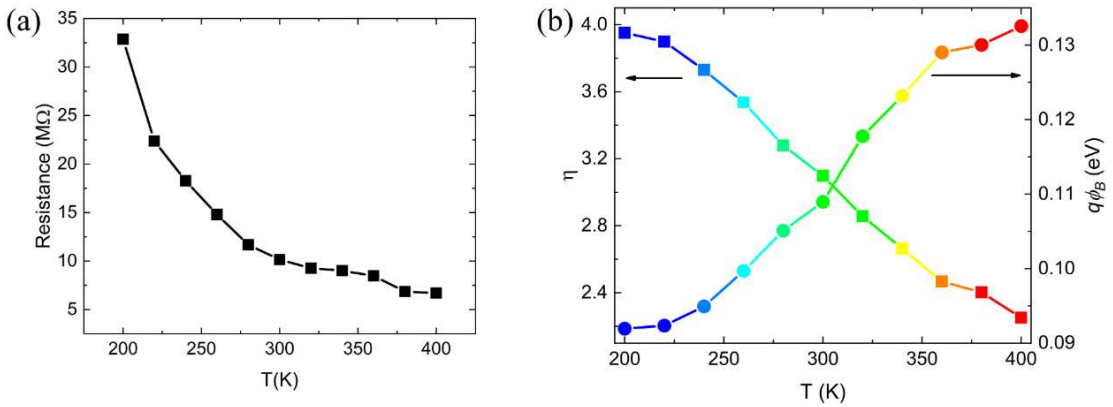


Fig. 48 (a) Devices series resistance, b) ideality factor and the Schottky barrier extracted from the C.C. method versus the temperature.

The exponential reverse current growth at lower temperatures in Fig. 45 can be explained considering the Fermi level shift due to the graphene low density of states, which reduces the Schottky barrier in reverse bias. In Fig. 49 (a) and (b) we show the Richardson plot at given forward and reverse biases. In forward bias, the temperature dependence of the current has a linear behaviour, which is in agreement with the T.E. theory. Contrarily, in reverse bias, the evolving behaviour of the current, from exponential to saturation trend, is reflected in the Richardson plot (Fig. 47 (b)), which for $T \leq 300K$ is similar to the forward bias one (Fig. 47 (a)), while at higher temperature shows rising converging curves. Because of this, we consider only the lower temperature part of the curves in Fig. 49 (b) ($T \leq 300K$) to determinate the Schottky barrier and the $\ln(AA^*)$, which are displayed in Fig. 49 (c). We highlight that the Schottky barrier increase with the applied voltage. In forward bias, the graphene Fermi level shifts down with respect to the semiconductor energy bands, thus increasing the Schottky barrier, while the opposite occurs in reverse bias. We also believe the variation of the barrier can be contributed by the geometry and doping level of the substrate through the image-force barrier lowering. The pillar geometry magnifies the electric field around the corner where a wider depletion layer is created. Such depletion layer is mirrored by charges in graphene, which cause an up-shift of the Fermi level and a reduction of the Schottky barrier. The high doping of the Si substrate can further contribute to barrier lowering through the image force effect [102]. Conversely, the change of behaviour at higher temperatures indicates that the augmenting thermal generation rate in the depletion layer dominates the reverse leakage current which become less sensitive to the bias. The slight deviation of such current from saturation can be ascribed to image force barrier lowering [28,32].

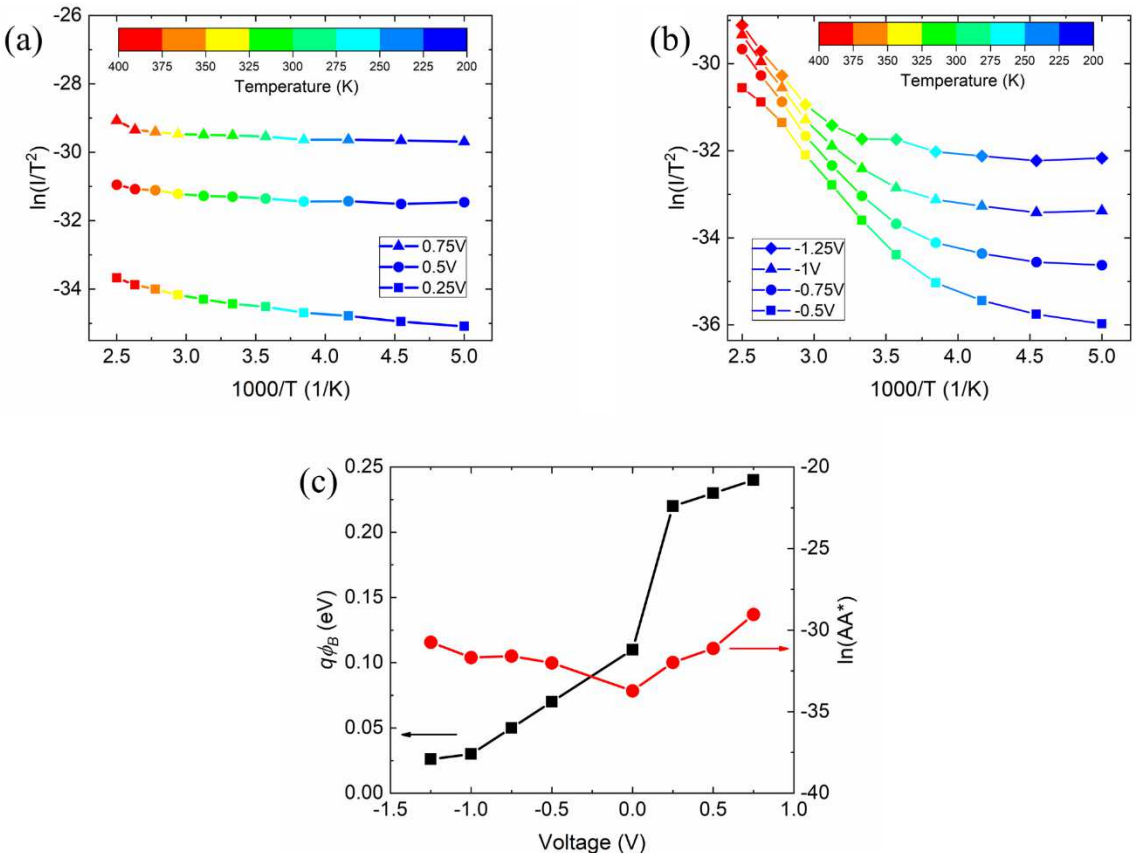


Fig. 49 a) Richardson plot of $\ln(I/T^2)$ vs $10^3\ T$ in forward and b) in reverse bias. c) Schottky barrier and $\ln(AA^*)$ respect the bias.

Because of the CMP treatment, there is a possibility that the pillar top surface is not homogeneous and there could be points where the Schottky barrier is higher or lower. Following ref. [123], we assume that the spatial variation of the Schottky barrier can be described by a Gaussian distribution. Therefore, the temperature dependence of the barrier is expressed as:

$$q\phi_B = q\phi_{BM} - \frac{q\sigma^2}{2kT} \tag{4.1}$$

where $q\phi_{BM}$ is the maximum Schottky barrier and σ is the standard deviation of the Gaussian distribution. σ characterizes the inhomogeneity of the Schottky barrier and can be extracted from a plot of $q\phi_B$ vs $1/2kT$ (Fig. 49 (d)). We obtain a $\sigma = 45\ meV$, which is lower than the ones reported in literature for CVD grown graphene. Since the graphene was CVD grown, the low standard variation can be considered as a remarkable advantage of the patterning of the substrate.

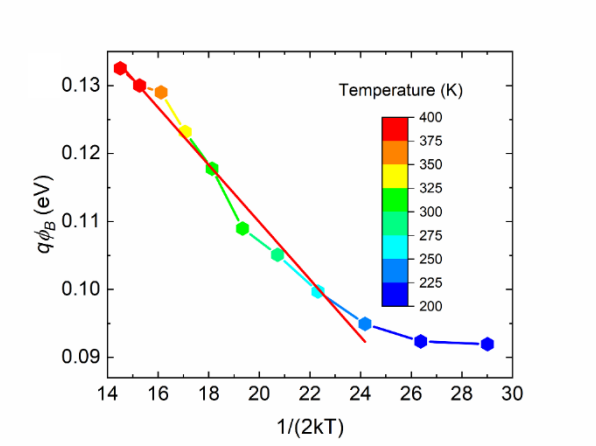


Fig. 50 Schottky barrier height at zero bias as a function of temperature.

Finally, we measured the Gr/Si-pillar response to light. Fig. 51 (a) shows the semi-logarithmic I-V curves of the device measured under different white LED light intensities. The responsivity $\mathcal{R} = \left(I_{light} - I_{dark}\right)/P_{opt}$ (I_{light} and I_{dark} are the current measured at $-1V$ under illumination and in dark, respectively) as a function of the incident light power P_{opt} is shown in Fig. 51 (b). The device presents a responsivity with a maximum of $\sim 88\ A/W$ at $10^{-5} - 10^{-4}\ Wcm^{-2}$, which decreases at higher intensities.

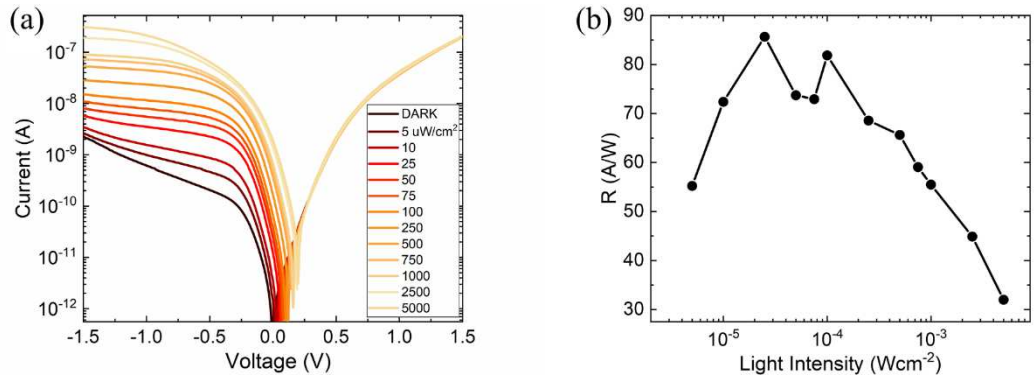


Fig. 51 a) I-V characteristic in semilogarithmic scale of the Gr/Si-pillar device measured at different intensity illumination level. b) Responsivity of the gr/Si pillar device as function of the light intensity

Indeed, at high illumination, the increasing of electron-hole pair density in the depletion layer enhances the recombination rate thus making the photocurrent deviate from its linearly behaviour as shown in Fig. 52 (a).

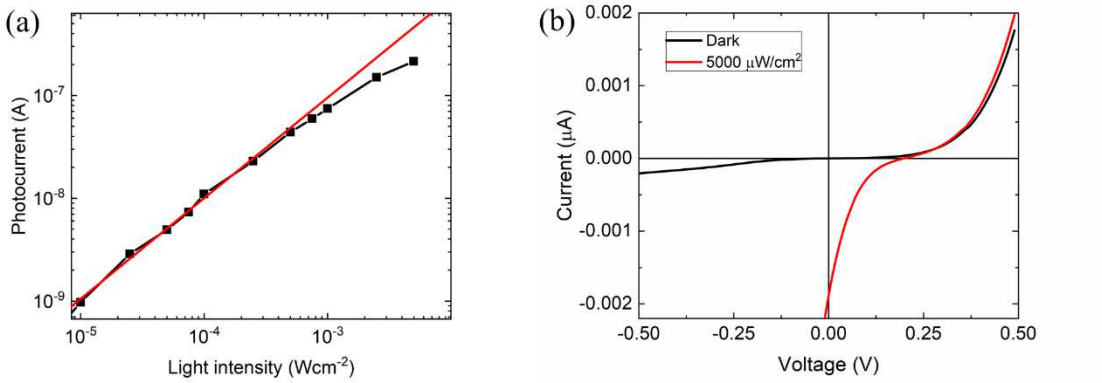


Fig. 52 (a) Gr/Si-pillar Photocurrent measured at $-1V$ and at different light intensities in logarithmic scale, (b) I-V characteristic measured in dark (black line) and at $5\ mWcm^{-2}$ (red line)

Remarkably, the device achieves a reverse current that can be greater than the forward one. The high reverse current measured at high illumination confirms that there is a contribution to the junction current from the photogeneration occurring in the substrate areas where graphene forms a MOS capacitor with Si, as explained in the previous chapter and ref. [27,29–34]. Furthermore, we note that the photogeneration has the same effect as the thermal generation in shaping the I-V curves of the device. Fig. 52Fig. 51 (b) shows the I-V measured in dark and under illumination at $5\ mW/cm^2$ in linear scale. A photovoltaic effect with an open circuit voltage around $0.19\ V$, which is close to the estimated Schottky barrier height, and a short circuit current of $1.8\ nA$, corresponding to ~0.7 % power conversion efficiency can be clearly observed. The conversion efficiency can be improved by lowering the doping of the Si substrate, which would result in an extended depletion layer for enhanced light absorption, and by reducing the shunt and series resistance that would increase the cell fill factor.

4.2 Graphene/Silicon-tip Junction

In the previous paragraph we observed that is possible to realize a bias tunable Schottky barrier by introducing a sharp geometry in the junction. In order to prove that, we patterned a matrix of tips on a silicon substrate and formed a Gr/Si-tip Schottky diode.

4.2.1 Gr/Si-tip Schottky Diode Fabrication

A matrix of tip (Fig. 53 (a)) was patterned on a highly doped Silicon substrate. The fabrication includes a SiO_2 or Si_3N_4 hardmask with photo-resist patterned by lithography, reactive ion etching of Si, plasma-enhanced chemical vapor deposition of a thick SiO_2 layer completely covering the formed Si-tips, and a CMP planarization step to remove the SiO_2 on the top of the tips. Before the transfer, the Si-tip substrate were dipped in a 0.5%HF solution for $10\ s$ to remove only the native oxide on the Si-tip. Graphene was transferred from commercially available Cu foils using a wet transfer method.

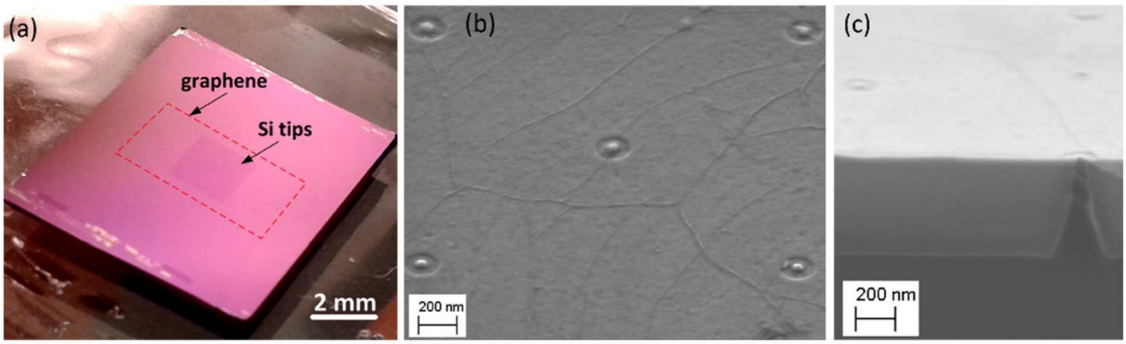


Fig. 53 (a) Photograph of a single chipwith a $2.5 \times 2.5\ mm^2$ *Si-tip array covered by amonolayer graphene transferred fromCu. (b) SEM top view of the tips emerging from the SiO2 insulating layer and covered by graphene. The diameter of the emerging tips is ~50 nm. Graphene wrinkles characteristic of graphene transferred from Cu are visible. (c) SEM cross-section image showing one of the Si-tips embedded in SiO2 and covered by graphene. The tip pich size is* $1.41\ \mu m$ *and the tip height is ~0.5* μm.

Fig. 53 (b) shows a scanning electron microscopy (SEM) image taken after graphene transfer: five silicon tips with a diameter of about $50\ nm$ are seen underneath the graphene layer and wrinkles, characteristic of CVD graphene grown on Cu, can be clearly identified. Fig. 53 (c) shows a SEM cross-section of one of the Si-tip with graphene.

The high-quality of the graphene layer has been investigated using Raman spectroscopy measurements with a $514\ nm$ laser (spot size $\sim 600\ nm$). Fig. 54 (a) shows a representative spectrum taken from an area between the Si-tips. The high peaks at $\sim 2700\ cm^{-1}$ (2D) and at $\sim 1600\ cm^{-1}$ (G) typically of the graphene, and the small peak at $\sim 1350\ cm^{-1}$(D) which is related to the defect, indicate that the graphene layer is of high-quality. As shown by peak intensity mapping measurements presented in Fig. 54 (b), the position of the D peak does not correlate with the position of the Si-tips. The observed local increase of the D band intensity is mostly related to the presence of multi-layered graphene islands. Similarly, no correlation between the $2D/G$ peak intensity ratio and the positions of the Si-tips was revealed (Fig. 54 (c)). The sheet resistance of the graphene layer measured using the 4-probe technique beyond the Si-tips was $\sim 0.9\ k\Omega/\square$, a value in the range typically reported for CVD graphene on Cu.

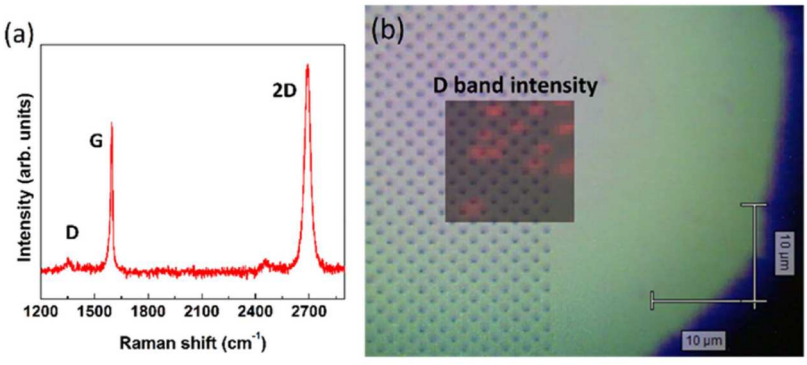


Fig. 54 (a) Representative µRaman spectrum taken after graphene transfer. (b) Dband intensity distribution extracted from Raman mapping measurement on an area of $12 \times 12\ \mu m^2$ *overlaid on optical image.*

The setup used for electrical measurements of the Gr/Si-tips is illustrated in Fig. 55 (a). The top graphene layer was contacted with evaporated Au, while ohmic contact with the

scratched bottom Si substrate was made with Ag paste. The measurements were performed using the same system described before in vacuum.

4.2.2 Electrical characterization

The dark I-V characteristic of the Gr/Si-tip Schottky diode in the temperature range $120 - 390\ K$ are shown in Fig. 55 (b). The device exhibits a rectifying behaviour of 3 order of magnitude. At modest positive bias, the room and higher temperature forward I-V curves show almost an ideal Thermionic emission behaviour. while at lower temperature, $T < 250K$, the forward bias current is dominated by a leakage component that adds a non-linearity to the semi-log I-V plot. These components are the recombination current and the tunneling. Such components become relevant when the low-temperature suppresses the thermionic emission, $T = 121\ K$, where it manifests in the interval $0 < V < 0.25\ V$.

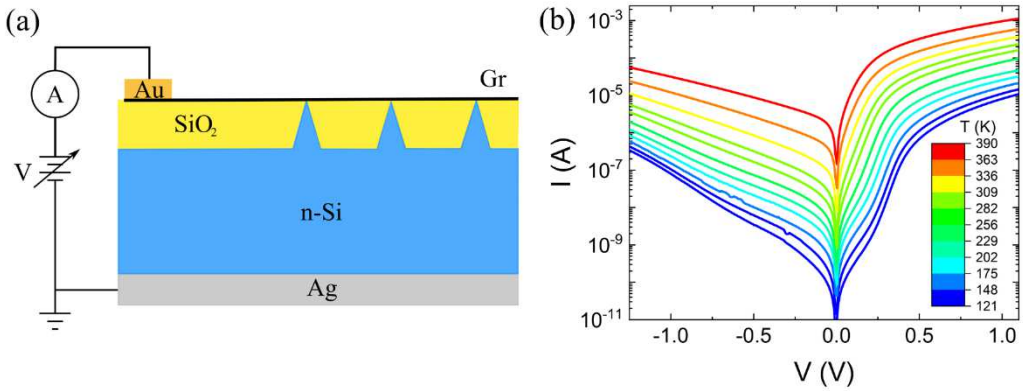


Fig. 55 (a) Layout and measurement setup of the Gr/nSi-tip device. (b) I–V characteristics in the temperature range 120–390 K and in steps of ~30 K measured in dark and at atmospheric pressure.

At reverse bias, the device exhibits an exponential growing current similar to the one we observed in the Gr/Si-pillar Schottky diode, but it does not saturate at higher temperature, which suggest the current due to thermogenerated charge is small enough to be neglected. Since the silicon tip and the pillar junctions differ only for the substrate geometry, this first result indicates that is possible to tune the Schottky barrier at even higher or lower temperature. In order to validate our theory, we determinate the Schottky parameters using the T. E. equations and the C.C. methods described in paragraph 2.6.

Fig. 56 (a) and (b) display the ideality factor η and the series resistance R_S respect the temperature obtained from both methods. Both shows a decreasing respect the temperature suggesting that also in this case the thermionic emission is the dominant transport mechanism. At room temperature the Gr/Si-tip junction possesses $\eta \sim 1.2$, which is the smallest one we observed in this research and also one of the smaller reported in literature [16].

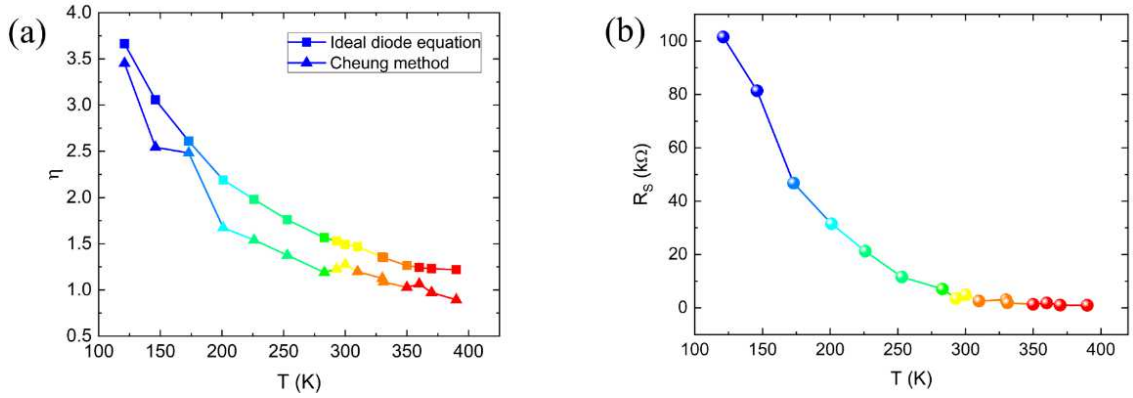


Fig. 56 (a) Ideality factor extracted from the T.E. and C.C. method and (b) series resistance.

Also, the R_S decreasing respect the temperature is similar to the other Gr/Si junctions R_S observed before. This behaviour has been attributed to the graphene layer [120–122]. In order to confirm the relation between the Schottky barrier variation and the geometry substrate we extrapolated the Schottky barrier at different bias.

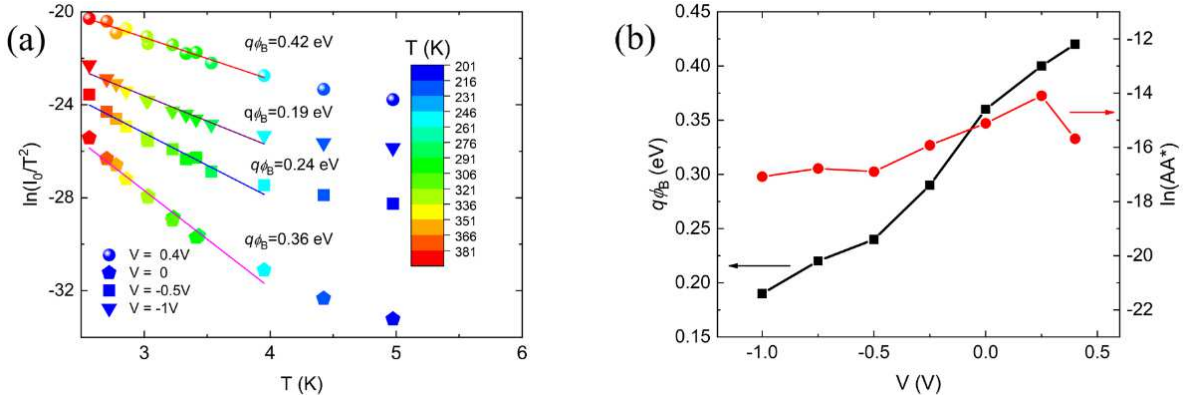


Fig. 57 (a) Richardson plot extrapolated and (b) Schottky barrier and $\ln(AA^*)$ at different bias.

Fig. 57 (a) shows some of the Richardson plot and Schottky barrier extrapolated at different bias, while in (b) are displayed the Schottky barrier and the $\ln(AA^*)$ respect the bias. We can observe an increasing of the Schottky barrier from negative to positive bias showing a value of $0.36\,eV$ at zero bias. Considering the average value of $\ln(AA^*) \approx -16$ and a junction surface of $6.075 \cdot 10^{-5}\,cm^2$ we can estimate a $A^* = 2 \cdot 10^{-3}\,A\,K^{-2}cm^{-2}$, which is lower than the typical value for Silicon but higher than the one we reported before [16]. As explained before, the low value of A^*, the temperature dependence of η as well the linear bias dependence of $q\phi_B$, can be ascribed to spatial inhomogeneities in the Schottky barrier height [123].

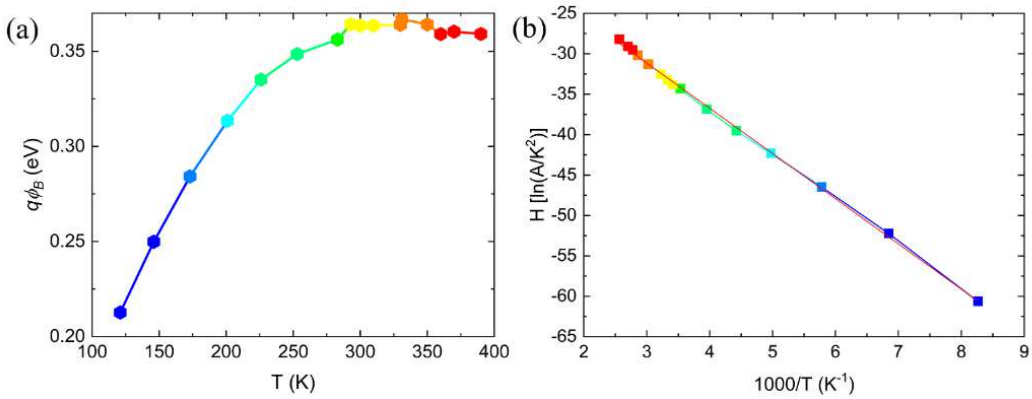


Fig. 58 (a) Schottky barrier measured at different and (b) modified Richardson plot according to the Gaussian distribution of the Schottky barrier height.

Since the Gr/Si-tip device under study is made of more than 3×10^6 nanojunctions, minimal tip-to-tip variation could result in significant barrier height fluctuations. Analogous to what we did for the Gr/Si-pillar, we measured the Schottky barrier height at zero bias at different temperature, Fig. 58 (a), using the C.C. method. Using equation (4.1) we obtained a Schottky barrier $q\phi_{Bm} = 0.47\ eV$ and $\sigma = 74\ meV$ which is in agreement with the value reported for Gr/Si planar junction. This result and the low ideality factor and the low Richardson constant, suggest that the tip geometry does not add inhomogeneity, but it seems to have the opposite effect.
From what we observed, the substrate geometry plays a major role in the Gr/Si junction electrical behaviour. The pillar and the tip geometry magnify the electric field around their corners and induce a potential which shift the graphene Fermi level. The reverse current exponential behaviour is the result of this shift [28]. The Gr/Si-tip junction possesses in fact a higher Schottky barrier, which is able to prevent the passage of high energy electrons.

The Schottky barrier height can be affected by different factors such as the lowering Schottky barrier effect and the presence of inhomogeneity like interfacial native oxide layer, traces of foreign materials or substances left from the transfer process [125,126]. Since the graphene layer, the silicon substrate and the transfer process are the same in both cases, we can assume that the Schottky barrier height is mainly affected by the native oxide layer thickness.
As we saw before, the presence of a thick oxide layer is also indicated by a high ideality factor. In this case, $\eta \sim 1.3$ at room temperature which suggest the presence of a thin oxide layer. By substituting the Richardson constant in equation (3.10), we obtain a thickness of $\delta \sim 6$ Å, which is the lowest value we observed in all the devices [16,27,29,32]. We believe that the low thickness layer is due to a lower time between the CMP and the graphene transfer.

4.2.3 Optical properties

We also studied the photoresponse of the Gr/Si-tip device by shining light from the top, on the graphene layer. Fig. 60 (a) compares the I–V curves obtained in darkness and under $3\ mW\ cm^{-2}$ white LED light; it shows clear photocurrent in reverse bias, and photovoltaic effect with $60\ nA$ short circuit current (a factor ~50 higher than the dark current at zero bias) and $70\ mV$ open circuit voltage.

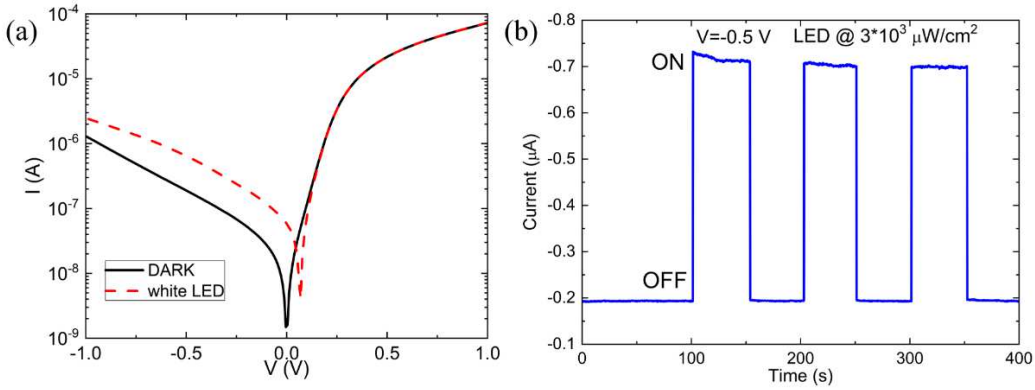


Fig. 59 (a) I–V characteristics of the graphene/Si-tip device in dark and under white LED illumination. (b) Current at V=−0.5 V in a sequence of light on/off cycles.

Fig. 59 (b) shows the stable photoresponse when the light is switched on and off, at a bias of $-0.5\,V$, corresponding to a responsivity $\mathcal{R} \approx 3\,A/W$. Fig. 60 (a) shows the photoresponse, at the same bias of $-0.5\,V$, to the near IR radiation produced by an 880 nm LED. The Gr/Si-tip device is expected to show high sensitivity around this wavelength, since Si has an absorption peak [102] at ~930 nm. The current plateaus of Fig. 60 (b) and of its top inset are the response of the Gr/Si-tip device to stepwise changes of electrical power fed into the irradiating diode. The radiation intensity in Wcm^{-2} reaching the Gr/Si-tip junction was measured to be $\leq 1\%$ of the IR diode supply power. Hence, Fig. 60 (b) shows that the minimum detectable IR intensity by the Gr/Si-tip heterojunction is less than $100\,mW\,cm^{-2}$ and its responsivity is $\mathcal{R}_{ph} \geq 0.3\,A\,W^{-1}$ at intensity $< 1\,mW\,cm^{-2}$. The measured responsivity is one or two orders of magnitude higher than the values reported to date for graphene/Si planar-junctions [33,34,127–130] (with maximum of $225\,mA\,W^{-1}$ at 488 nm) [35]. The graphene/Si-tip device appears also competitive when compared to semiconductor photodiodes on the market, whose typical responsivity is around $0.5\,A\,W^{-1}$, both for visible and near IR light. The high substrate doping reduces the space-charge region where most of the photoexcitation takes place and this should suppress the responsivity. This loss can be counterbalanced by the textured surface, which on the contrary favours multiple reflections and light absorption [131]. However, the high value of responsivity is rather a result of the peculiar device geometry. The tip enhanced electric field, other than facilitating their separation, can provide photogenerated electron-hole pairs with enough kinetic energy to cause impact ionization and initiate charge multiplication, thus enabling device internal gain. The exponential increase of the photocurrent with reverse bias can be taken as signature of internal gain since smoother rise is usually observed when the photocurrent is due only to increased photon absorption in the bias-widened depletion layer. Augmented photocharge separation and multiplication is also expected in graphene, especially in the areas near the tips. We notice that very high responsivity of $10^7\,A\,W^{-1}$ have been reported by Liu et al [132] in more complex three-terminal Gr/Si devices with quantum gain due to photocarriers borrowed into graphene and reinvested several times in the external circuit during their lifetime. However, these devices require more complex circuitry than our multi-purpose two-terminal photodiode.

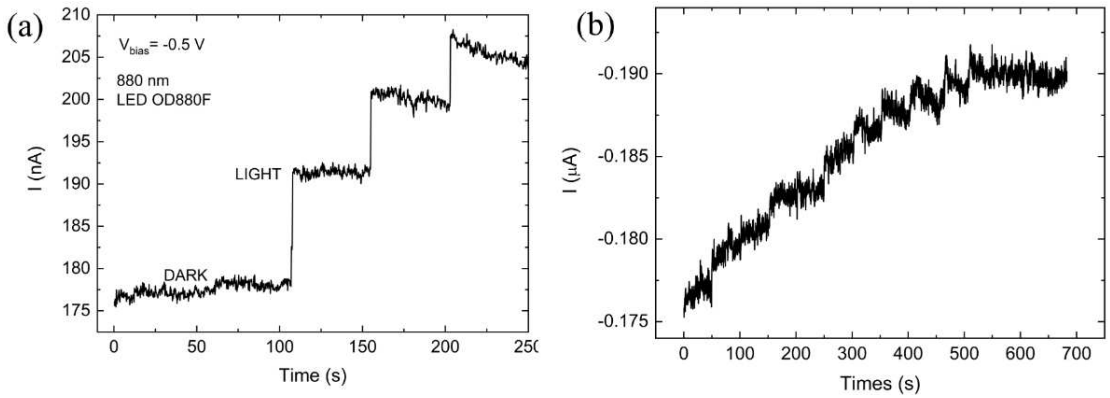


Fig. 60 (a) Reverse current at V=−0.5 Vunder 880 nmIR irradiation, increased in time by stepwise changes of the input electrical power to the emitting diode (OD880F). (b) displays the monotonic increase of the photocurrent of the graphene/Si-tip device while the IR diode input power is changed in smaller steps.

5 Conclusion

In conclusion, we fabricated and analysed four Gr/Si junctions, which differ for the type and doping concentration and substrate geometry. The Gr/Si flat junction shows to be the best approach to realize high sensible photodetector and can be also used as photovoltaic cell. Thanks to the small oxide thickness, the Gr/SiO_2/Si forms a MOS capacitor which is connected in parallel with the Gr/Si Schottky diode. The MOS attracts the photogenerated charges in the layer between the SiO_2 layer and the Si substrate creating a reservoir of charges which gives further contribute to the photocurrent of the Gr/Si Schottky diode. This discovery shows the potential of the Gr/Si junction as photodetector. Also, the type of the silicon doping affects the Schottky barrier. We observe that the Gr/n-Si diode possesses a higher Schottky barrier than the Gr/p-Si one. The Gr/p-Si low Schottky barrier has been explained by considering the graphene p-doped behaviour when it is exposed to the atmosphere. The graphene Fermi level is below the Dirac point and it is close to the silicon's valence band forming a small Schottky barrier. We also observe a performance degradation when the device is exposed to high temperature. The boron atoms diffuse from the silicon and p-dope graphene, thus further reducing the Gr/p-Si Schottky barrier.

We have also demonstrated that it is possible to tune the Schottky barrier height by patterning the substrate. The formation of sharp geometry close to the Gr/Si junction magnifies the electric field close to the junction; this induces a potential which shifts up (or down) the graphene Fermi level and decreases (or increases) the Schottky barrier. Also, it reduces the presence of inhomogeneity that could affect the junction I-V characteristics.

Although the Gr/Si junction possesses a high leakage, it seems to be promising as solar cells and photodetector. The possibility to tune the Schottky barrier could be used to create a cheaper and high sensible tuneable photodetector able to detect different light wavelengths by simply changing the bias. This research is not yet finished, there are a lot more of opportunities that this junction offers.

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